

FIG. 1

09/27/60

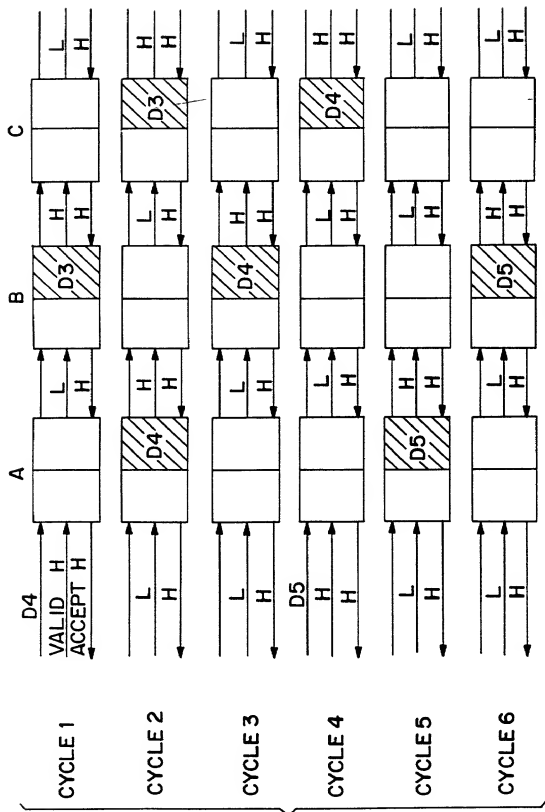


FIG. 2(A)

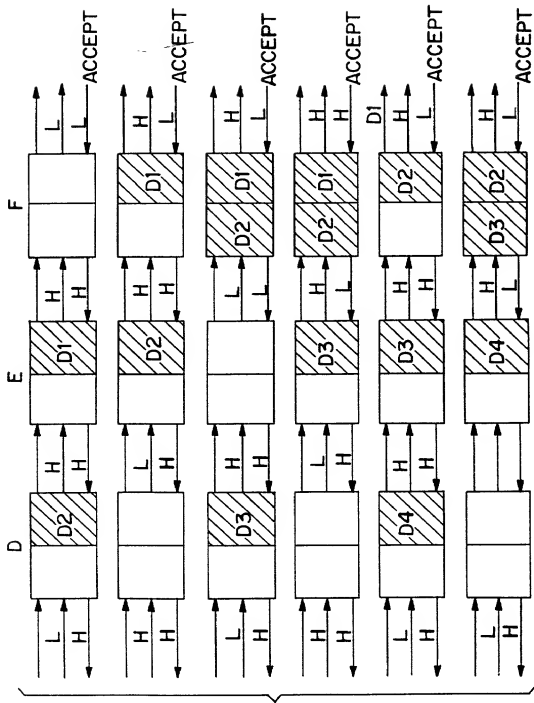


FIG. 2(B)

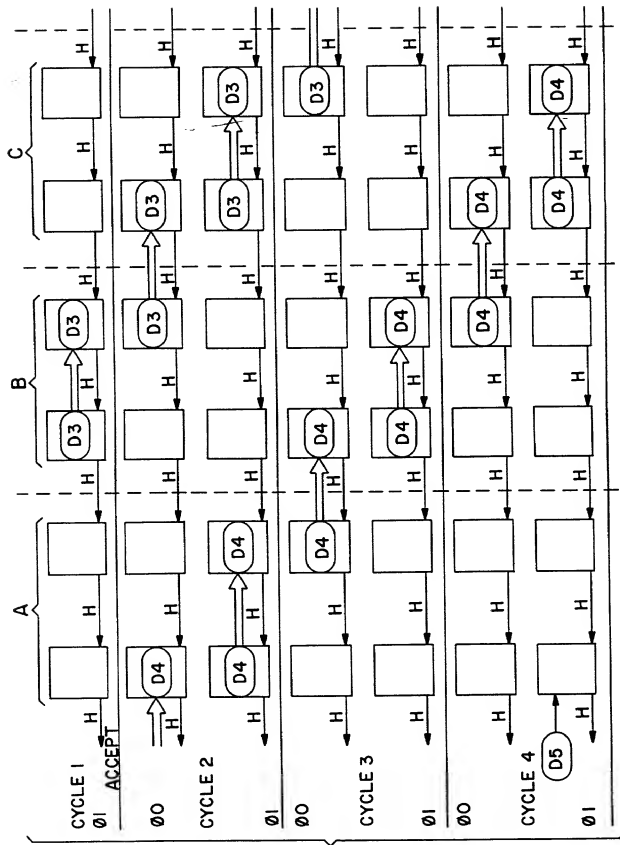


FIG. 3A-1

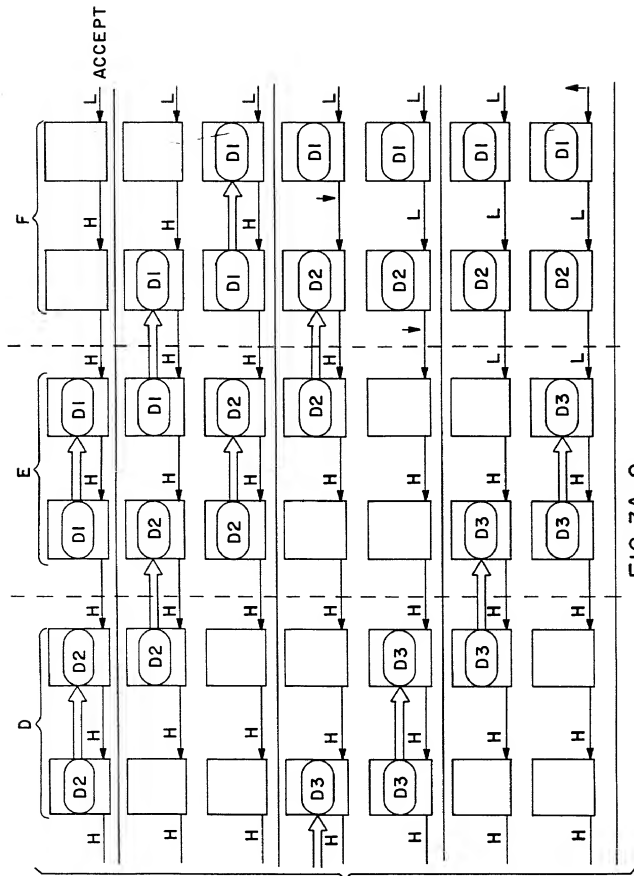
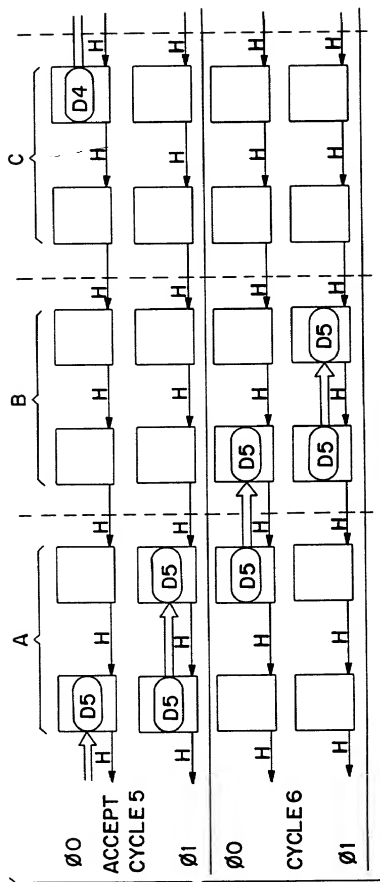


FIG. 3A-2



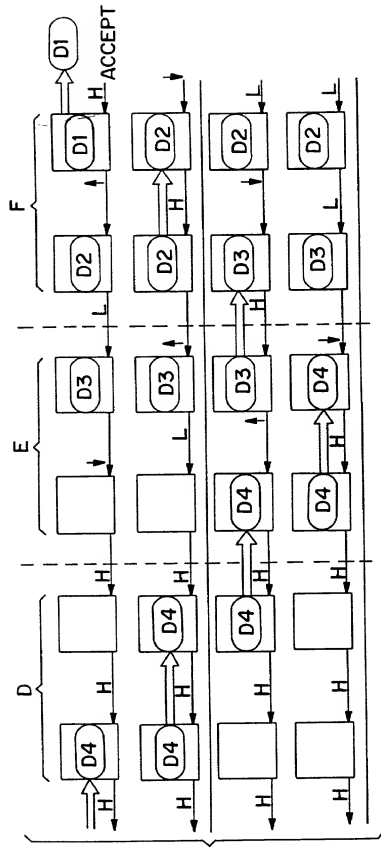


FIG. 3B-2

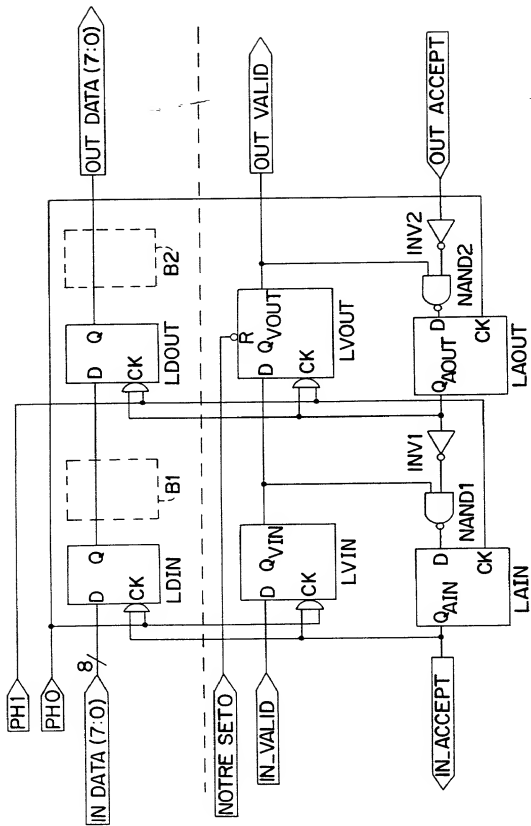


FIG. 4

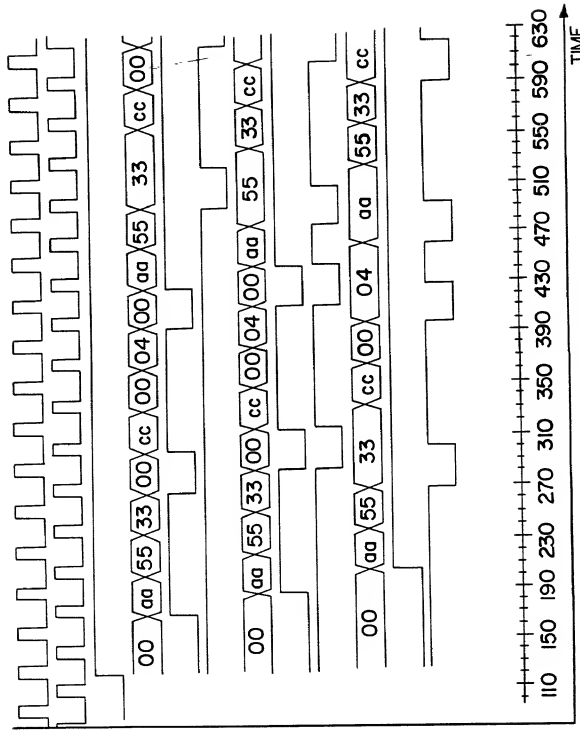


FIG. 5(A)

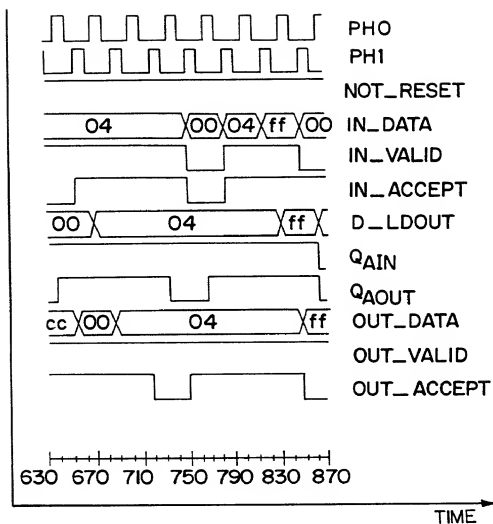


FIG. 5(B)

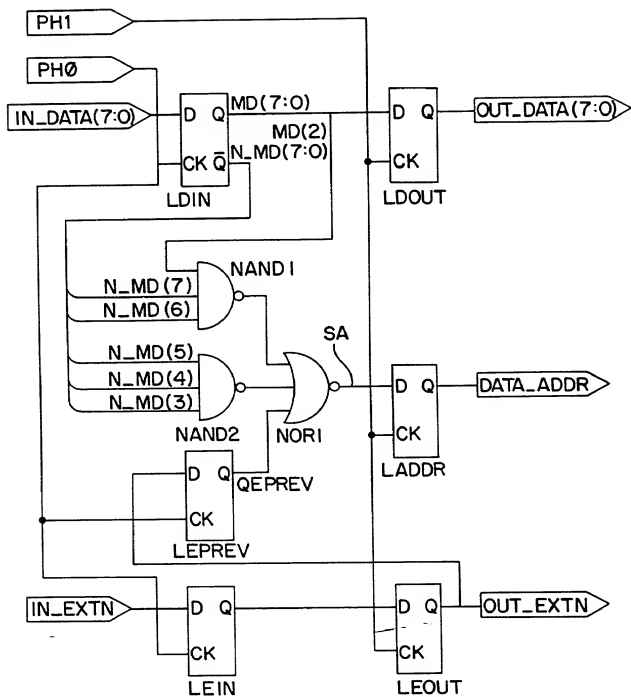


FIG. 6

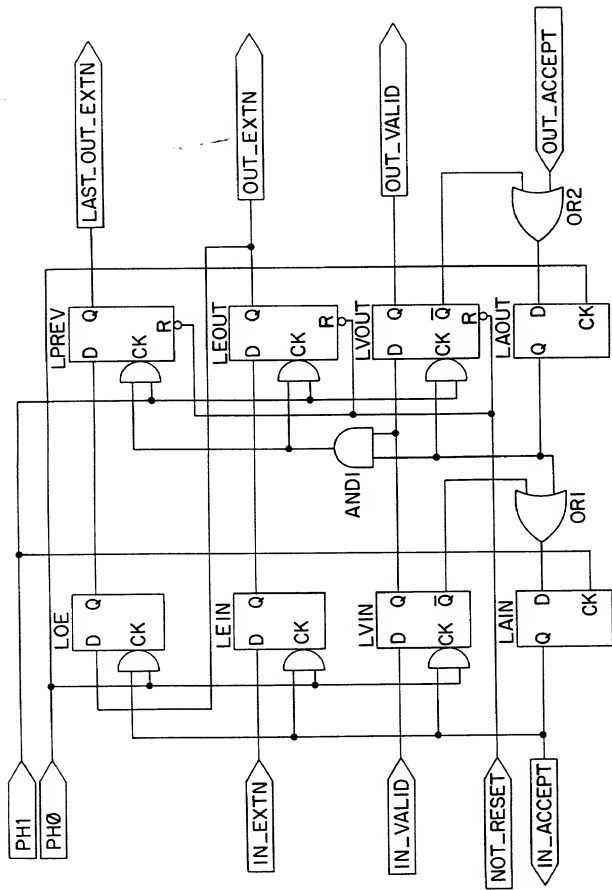


FIG. 7

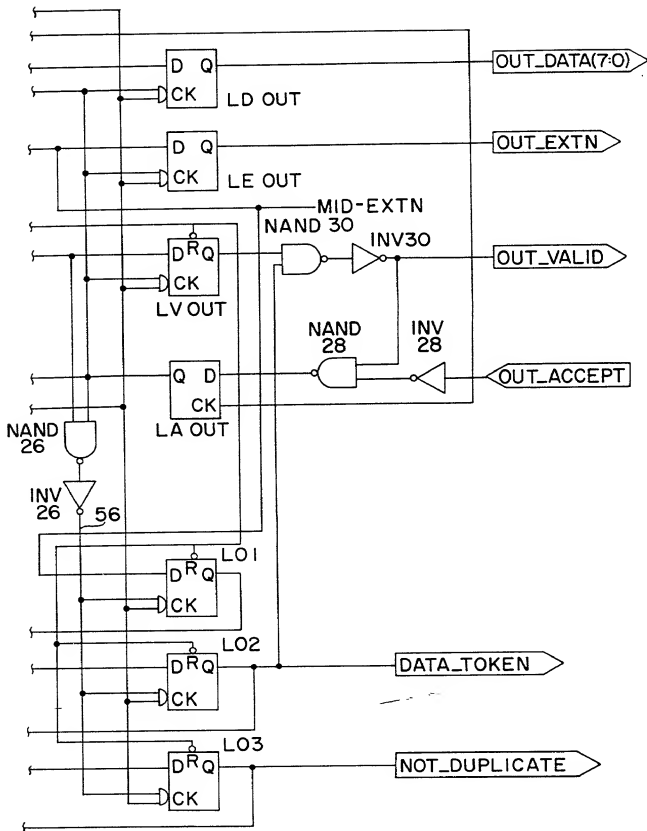


FIG. 8(B)

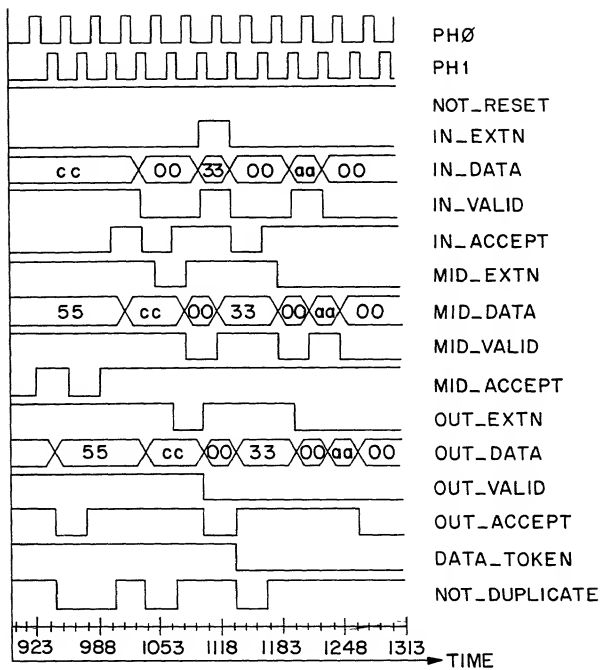


FIG. 9(B)

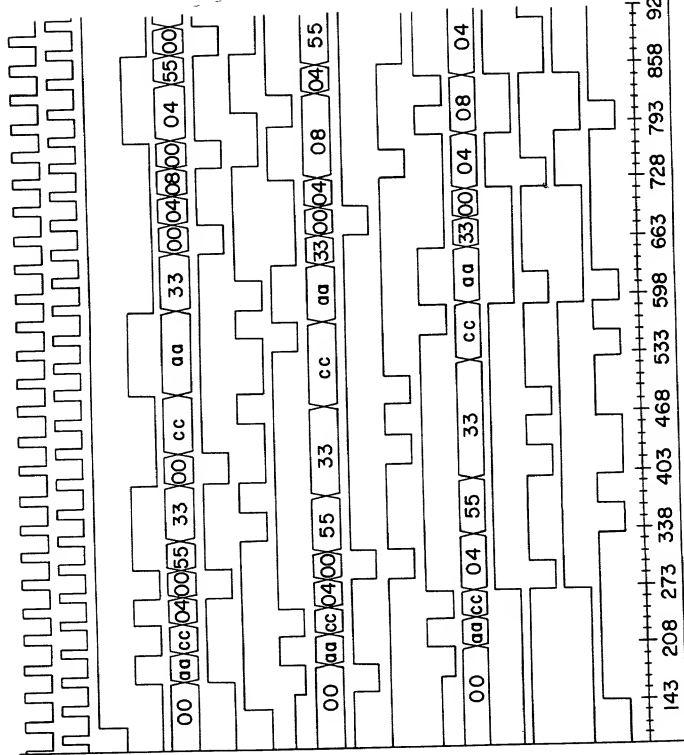


FIG. 9(A)

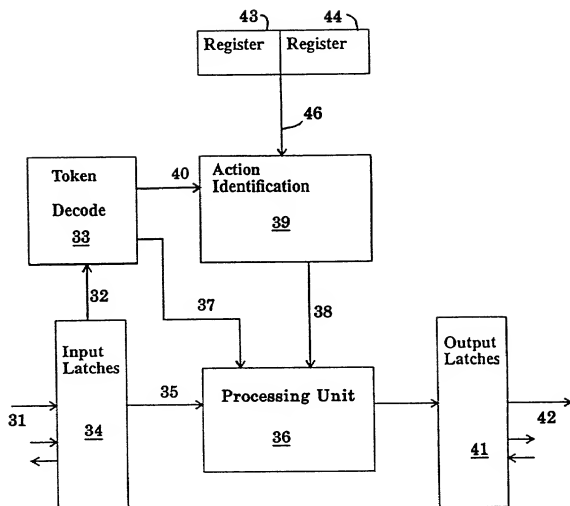
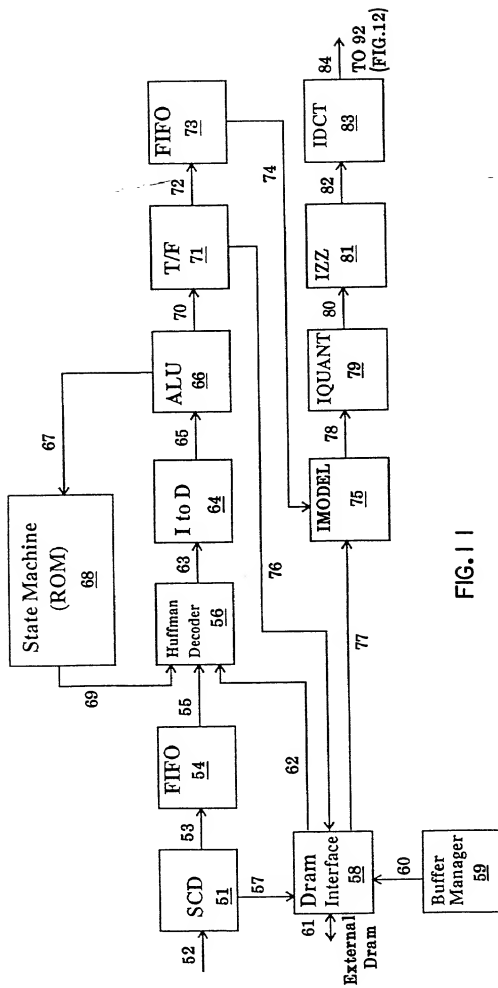


FIG. 10



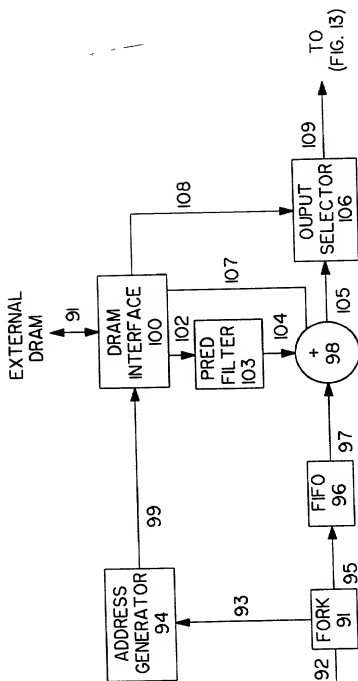


FIG. 12

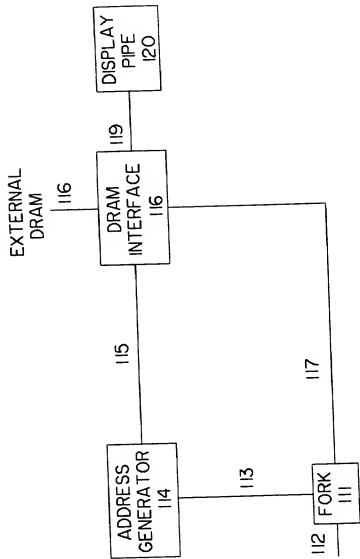


FIG. 13

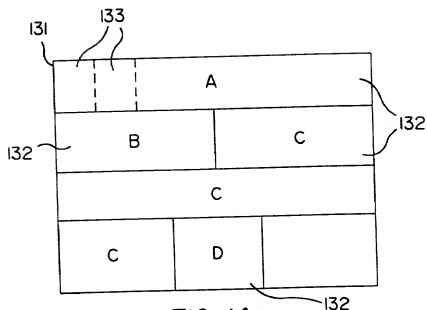


FIG. 14a

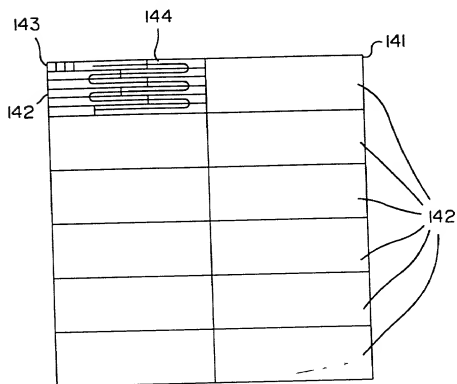


FIG. 14b

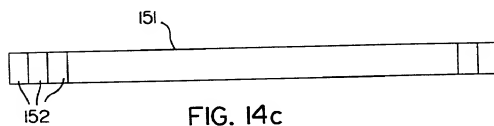


FIG. 14c

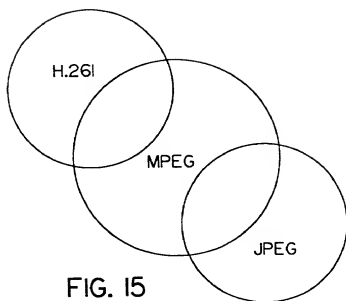


FIG. 15

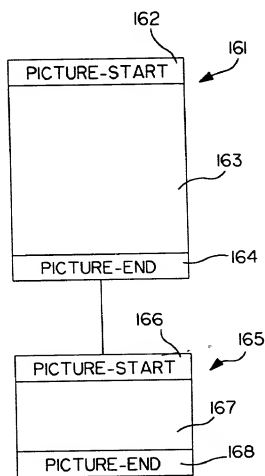


FIG. 16

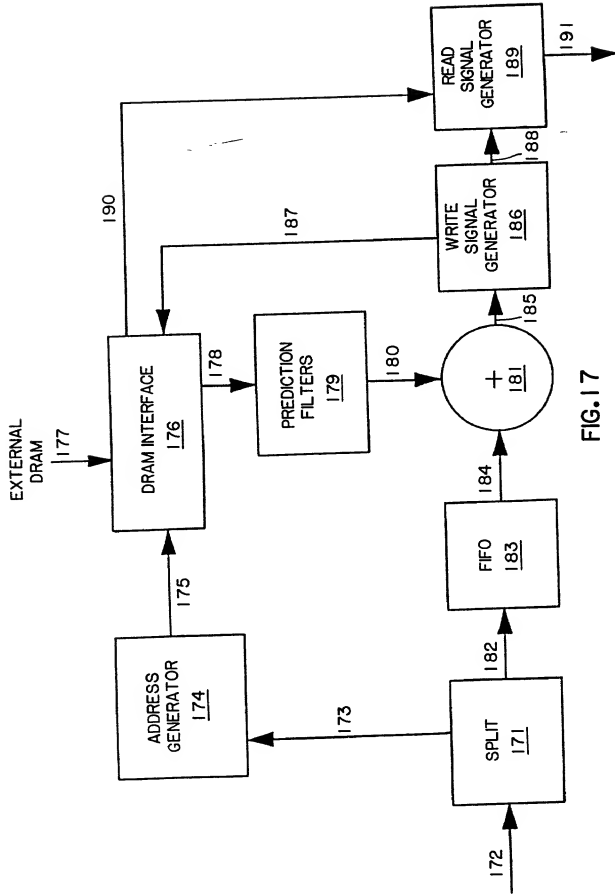


FIG. 17

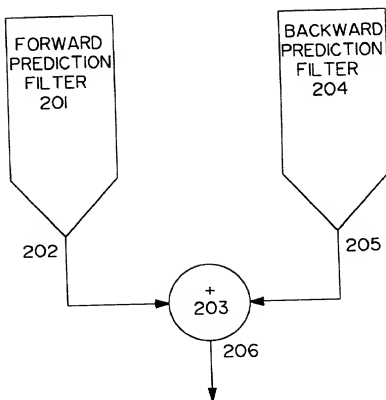


FIG. 18

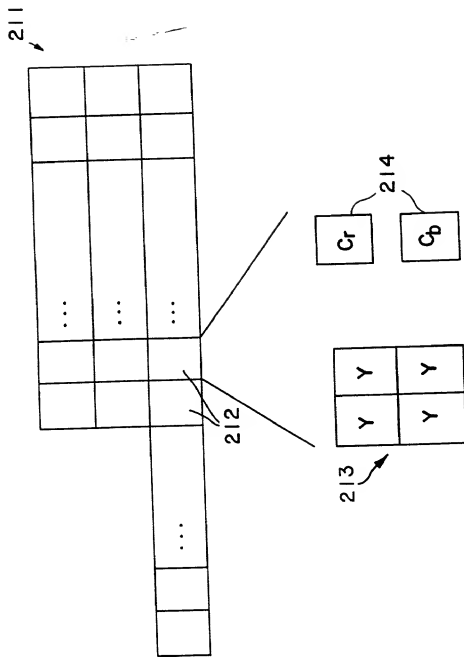


FIG. 19

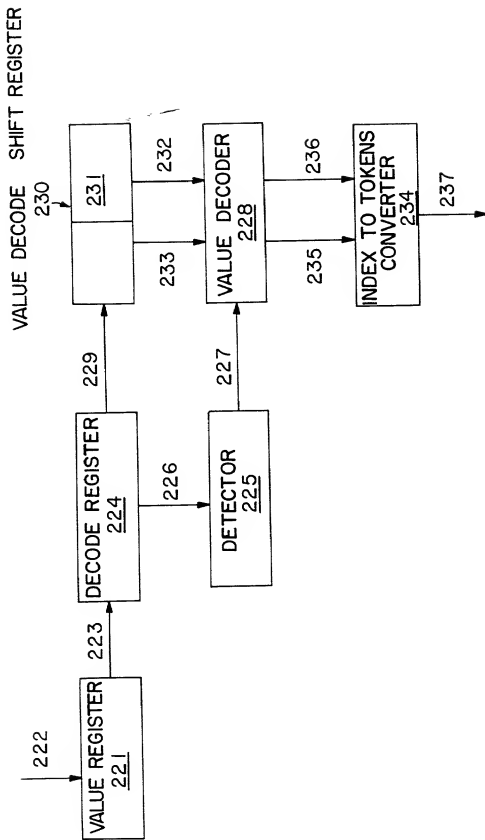


FIG.20

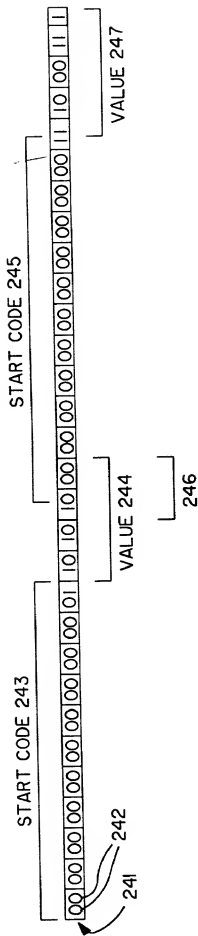


FIG. 21

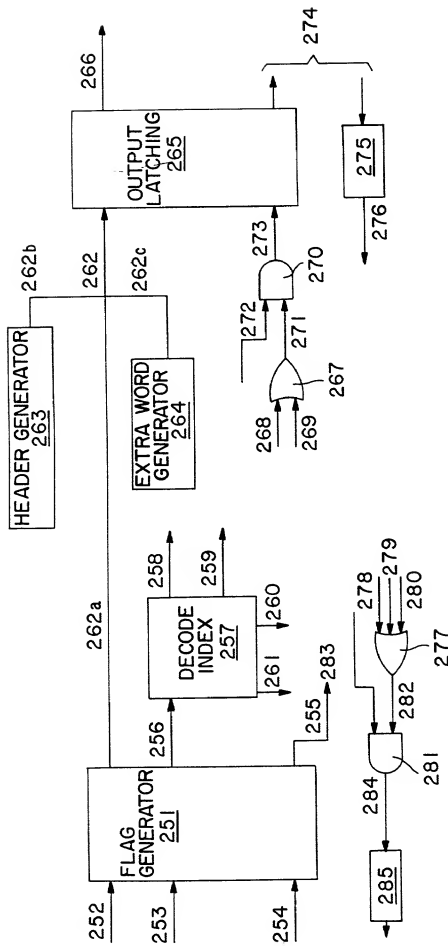


FIG. 22

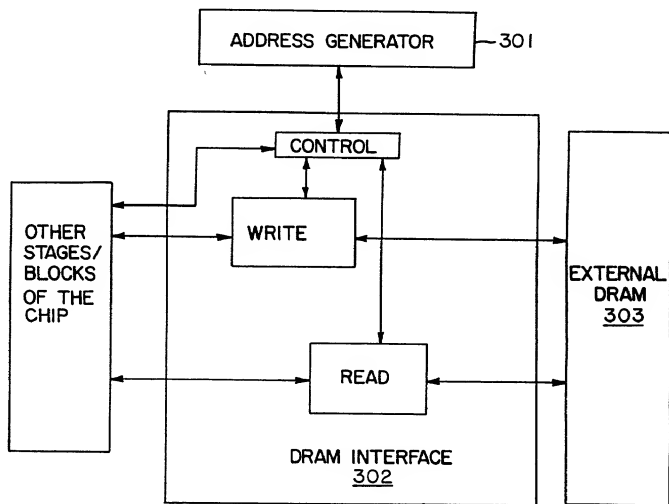


FIG. 23

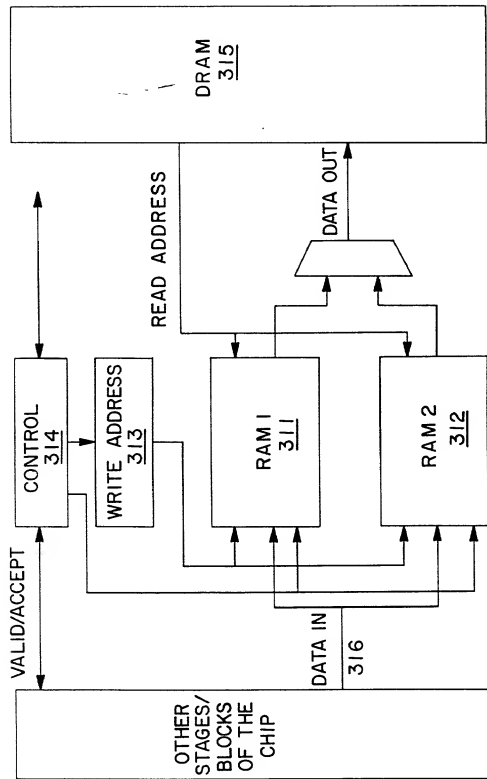


FIG.24

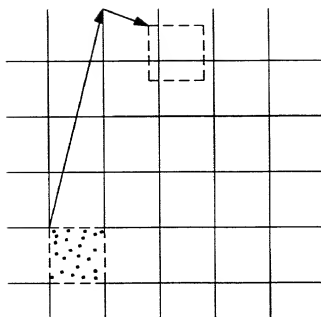


FIG. 25

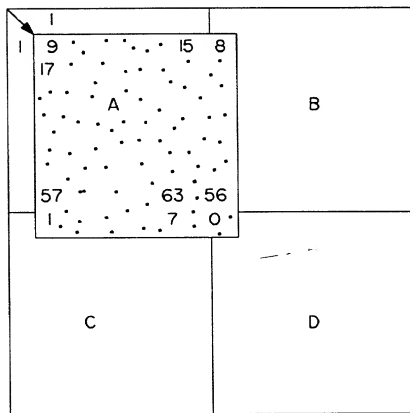


FIG. 26

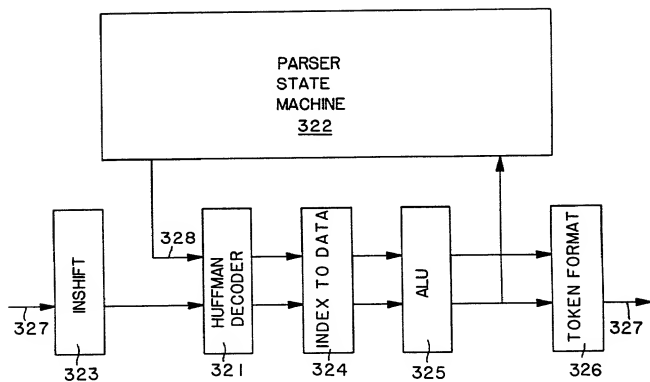


FIG.27

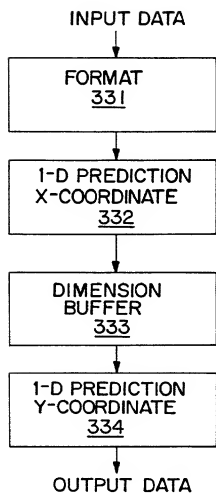


FIG.28

Multiplexed audio/video data

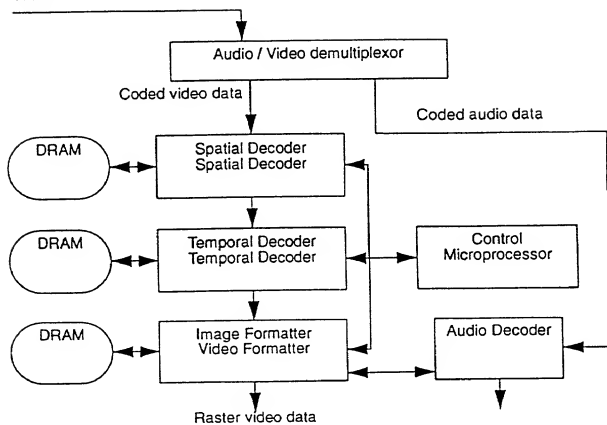
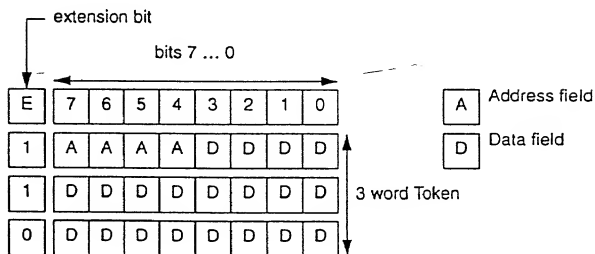
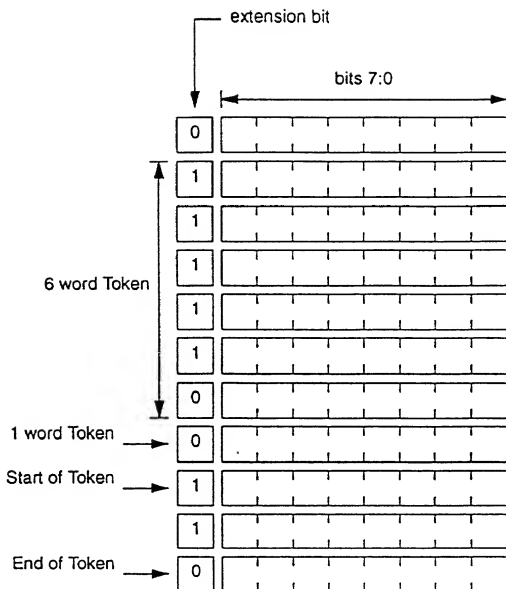


FIG.29



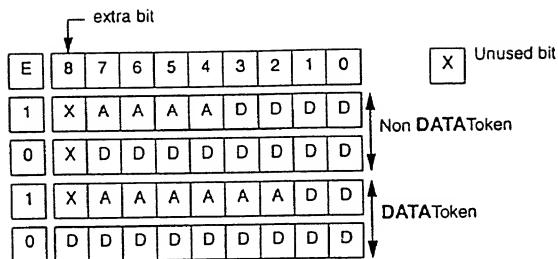
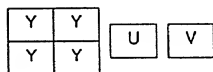
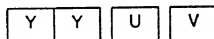


FIG.35



MPEG 4:2:0
macroblock

FIG.36A



JPEG 2:1:1
macroblock

FIG.36B

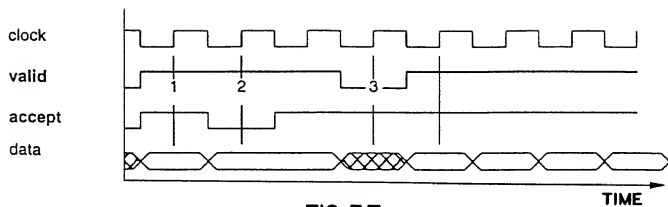


FIG.37

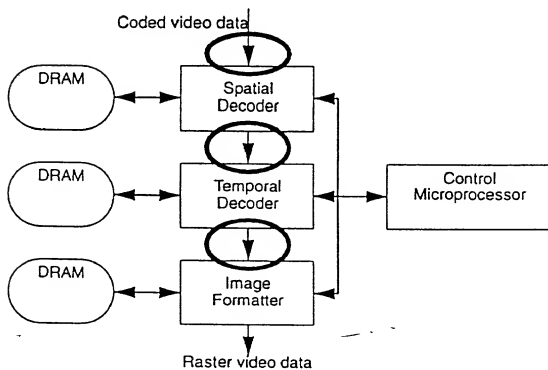


FIG.38

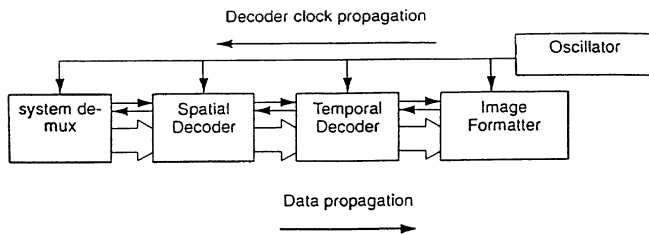


FIG.39

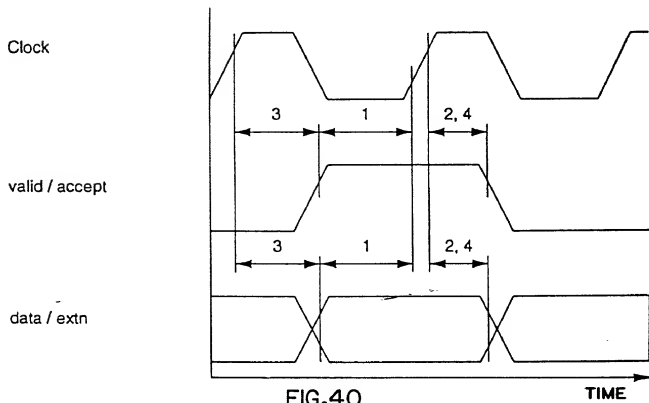


FIG.40



FIG.4 I

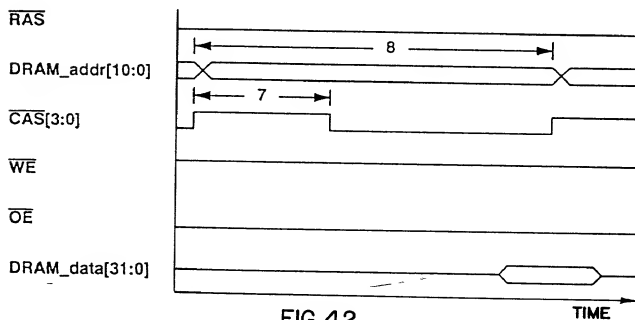


FIG.42

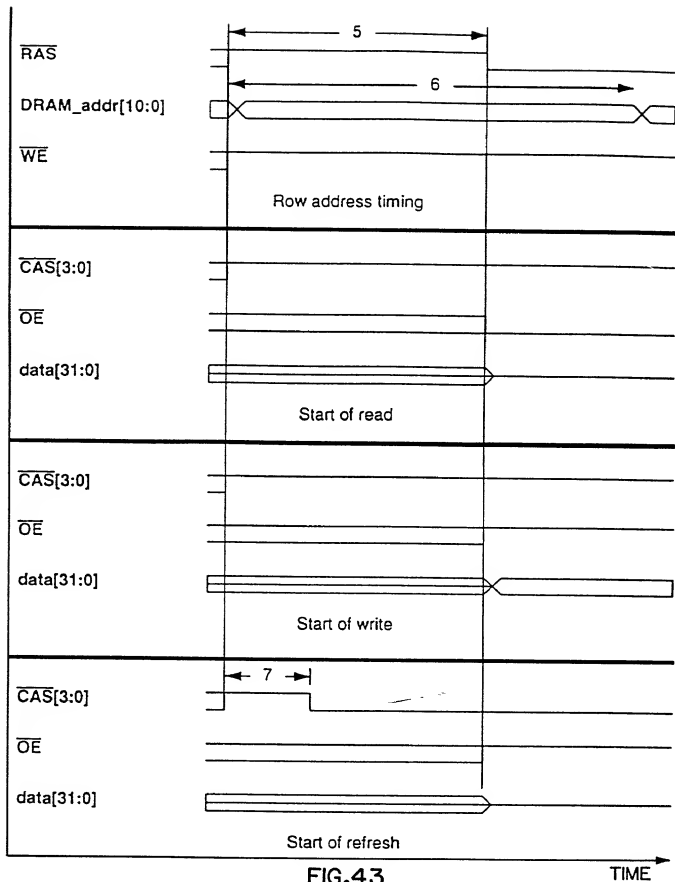
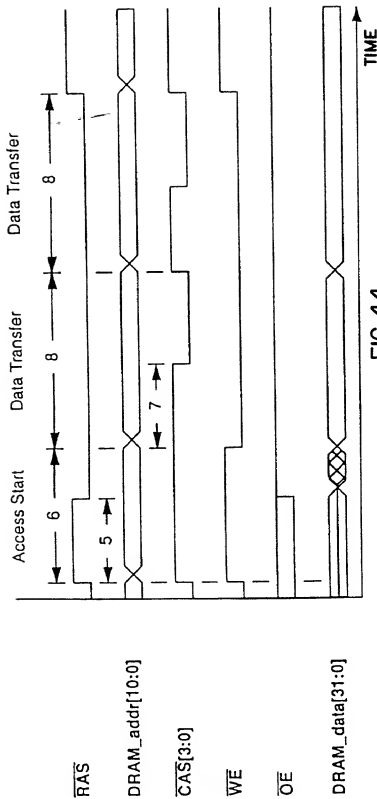


FIG.43



\overline{RAS}

DRAM_addr[10:0]

$\overline{\text{CAS}}[3:0]$

WE

OE

DRAM_data[31:0]

FIG.45

TIME

RAS

DRAM_addr[10:0]

CAS[3:0]

WE

OE

DRAM_data[31:0]

FIG.46

TIME

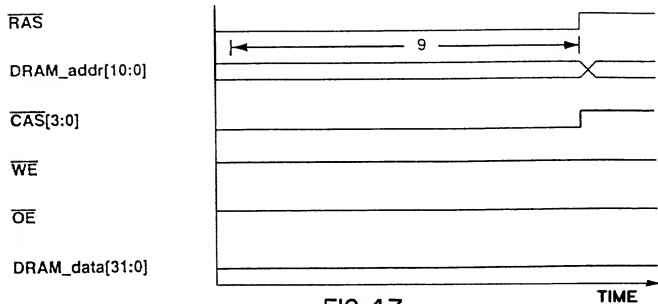


FIG.47

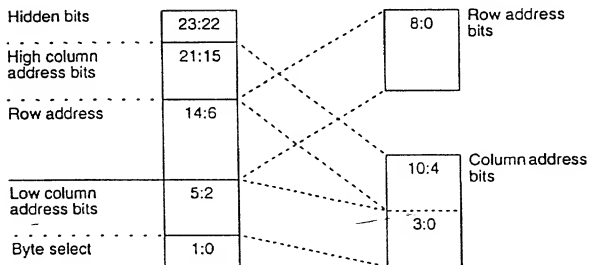


FIG.48

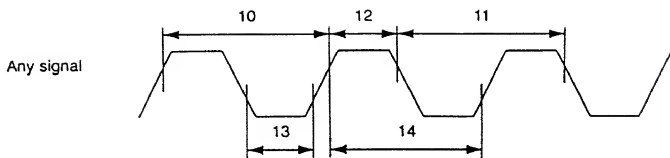


FIG.49

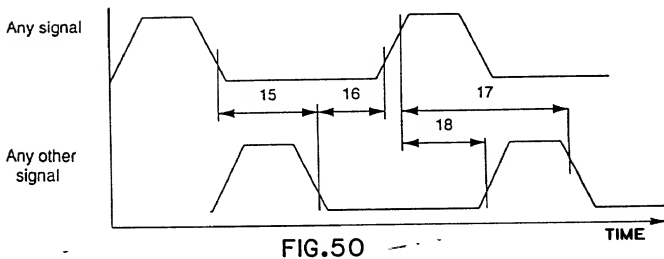


FIG.50

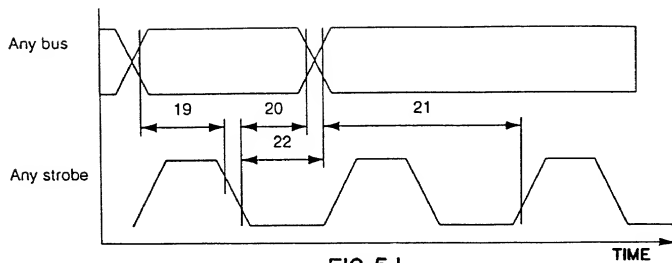


FIG.51

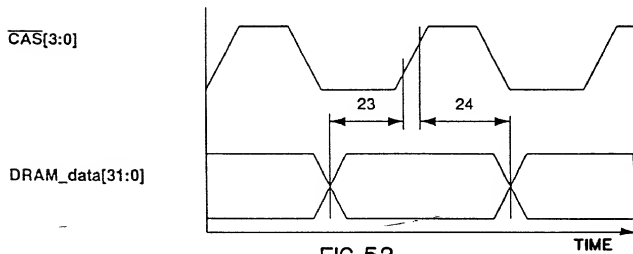
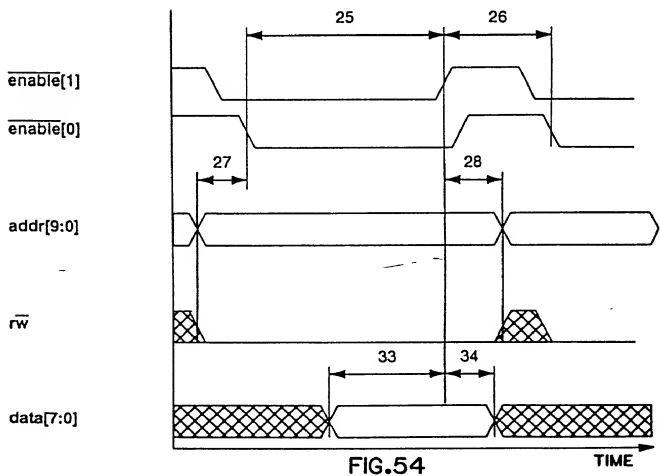
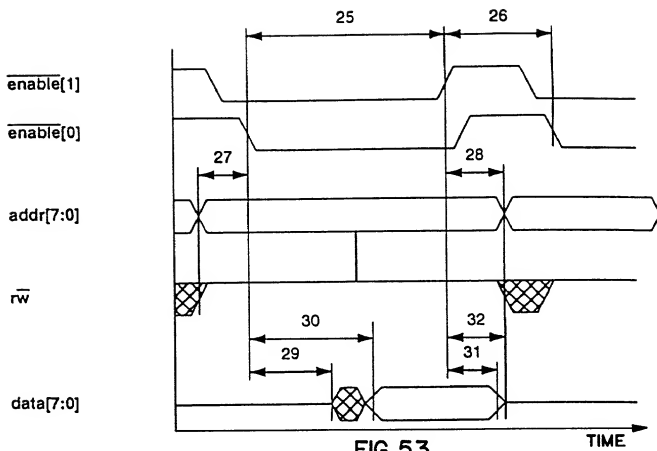


FIG.52



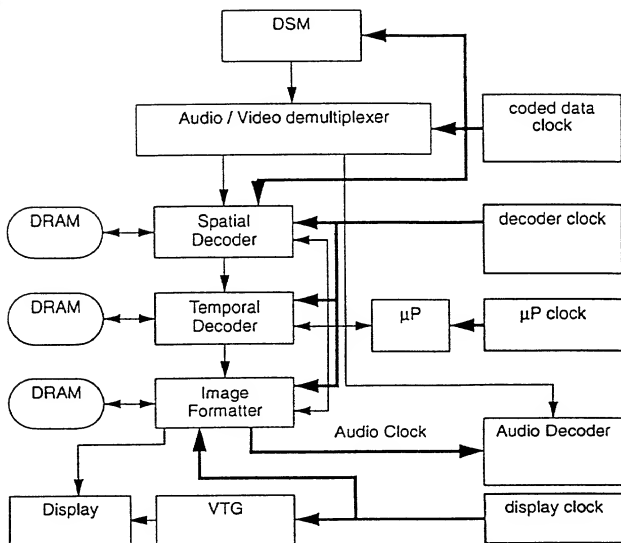


FIG. 56

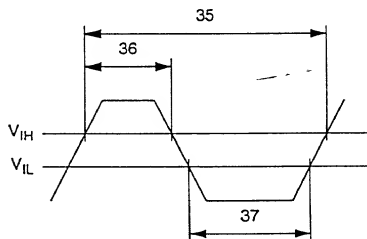


FIG. 57

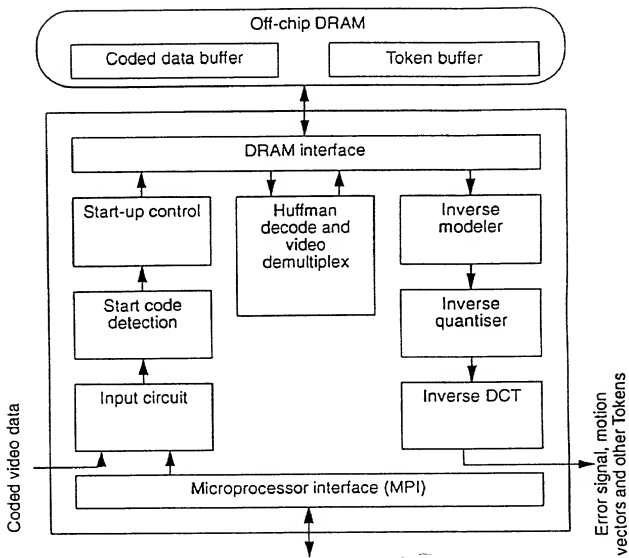


FIG.58

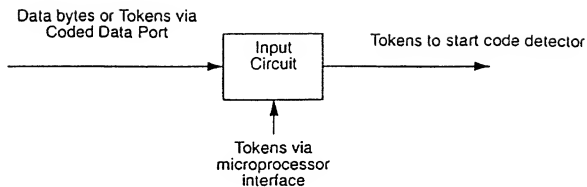


FIG.59

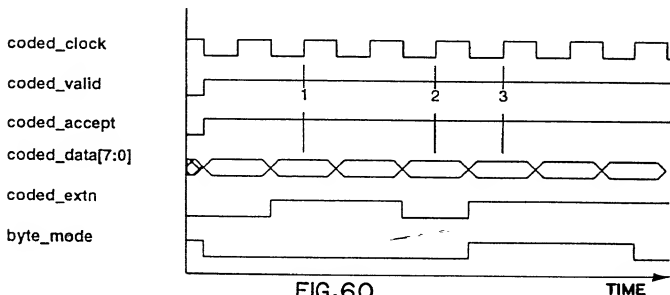


FIG.60

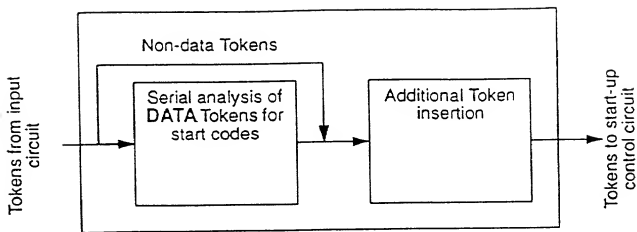


FIG. 61

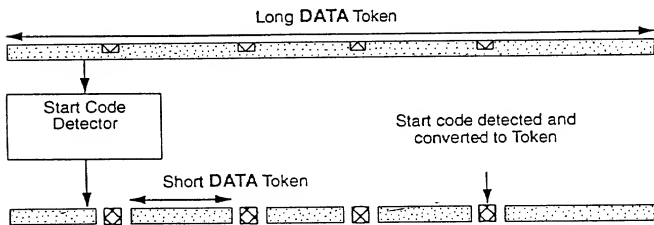


FIG. 62

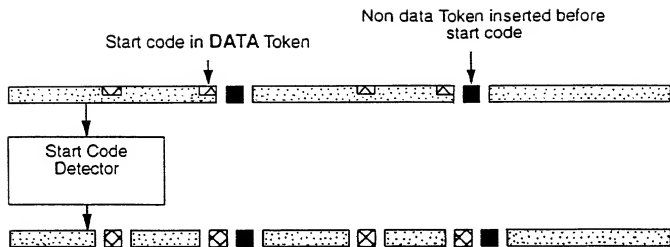


FIG.63

This looks like an MPEG picture start

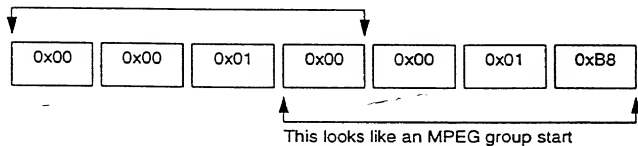


FIG.64

This looks like an MPEG slice start (0x28)

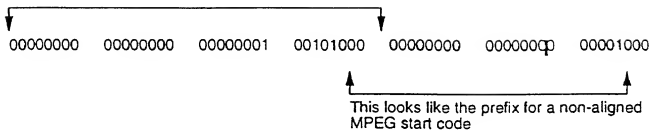


FIG.65

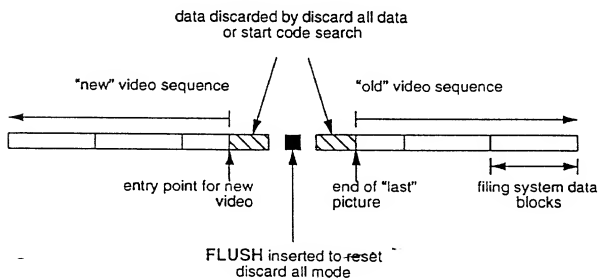


FIG.66

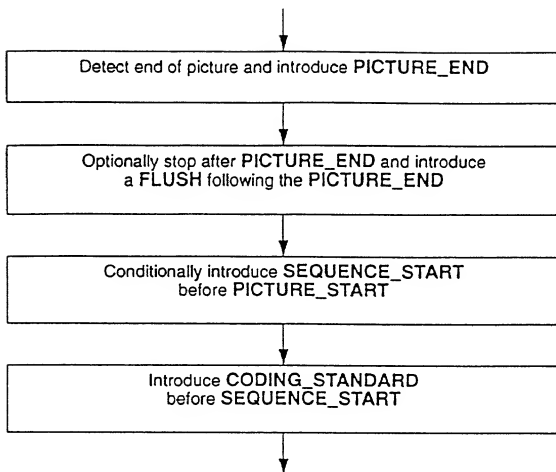


FIG.67

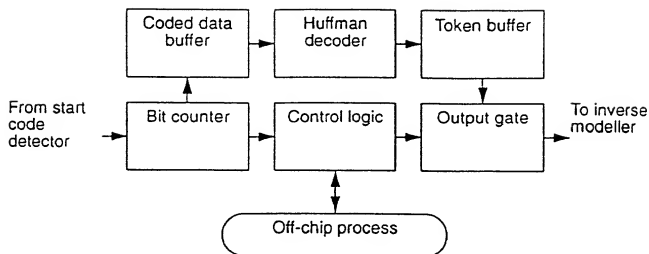


FIG. 68

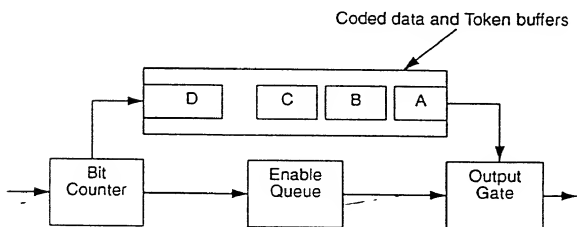


FIG. 69

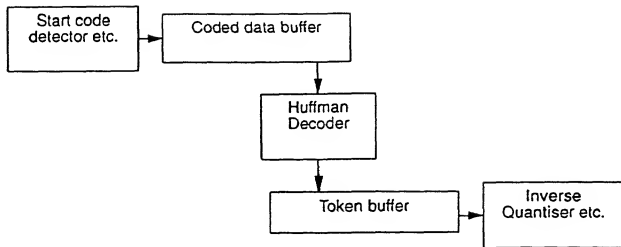


FIG.70

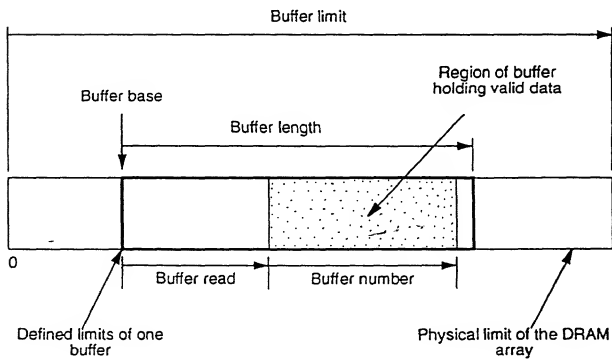


FIG.71

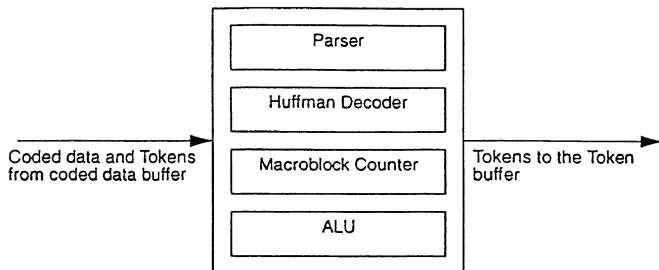


FIG.72

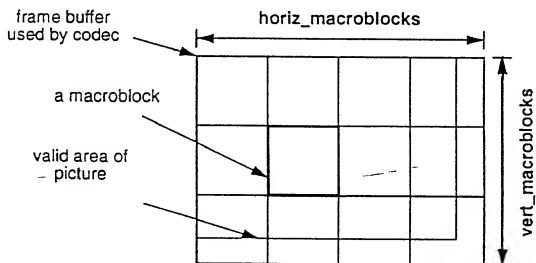


FIG.73

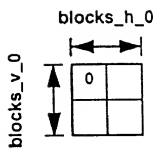


FIG.74A

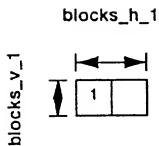


FIG.74B

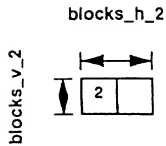


FIG.74C

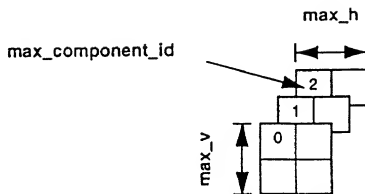


FIG.74D

$$\left\{ \begin{array}{l} \text{horiz_macroblocks} = \frac{\text{horiz_pels} + 15}{16} \\ \text{vert_macroblocks} = \frac{\text{vert_pels} + 15}{16} \end{array} \right.$$

FIG.75

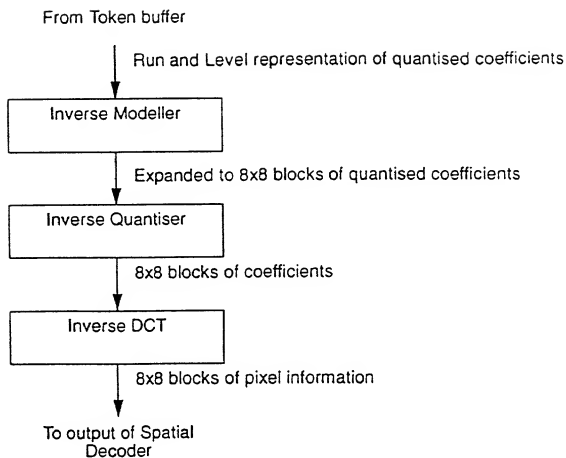


FIG.76

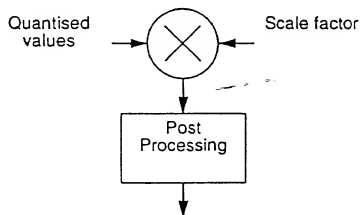
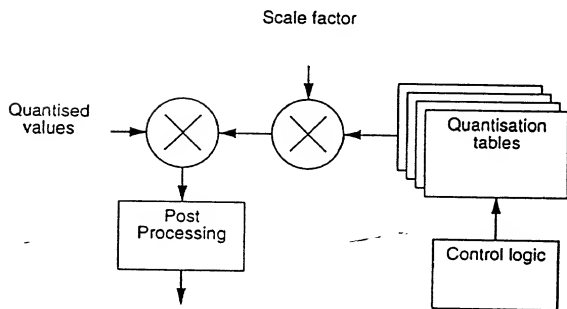


FIG.77



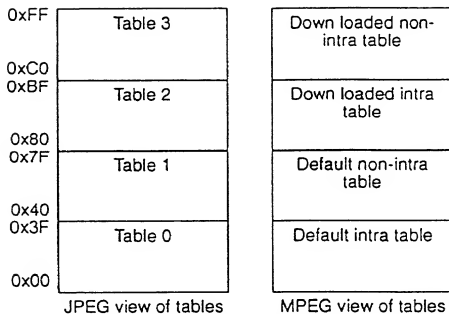


FIG.80

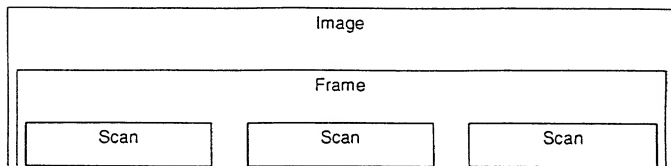


FIG.81

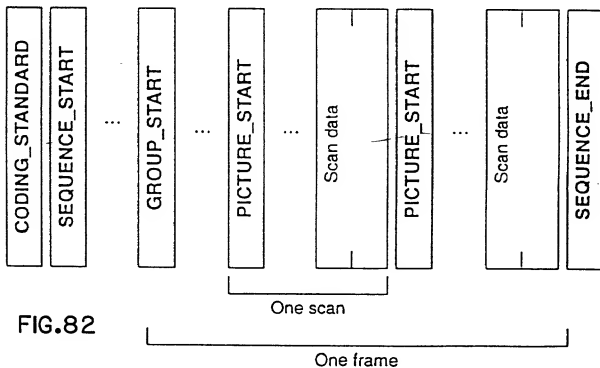


FIG.82

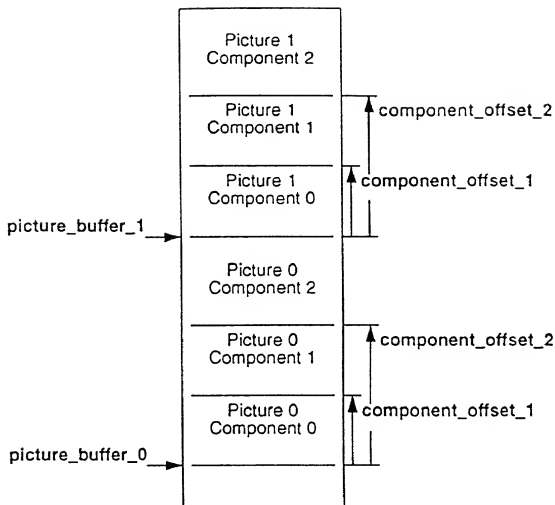


FIG.84

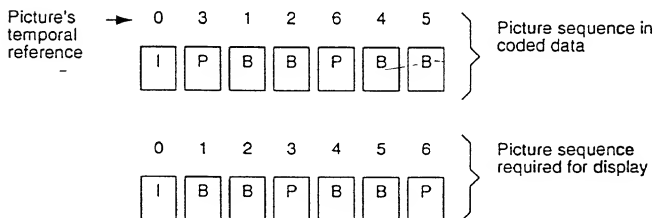


FIG.85

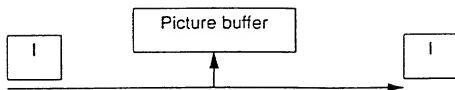


FIG.86

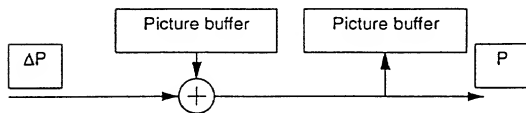


FIG.87

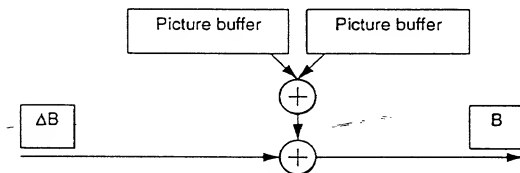


FIG.88

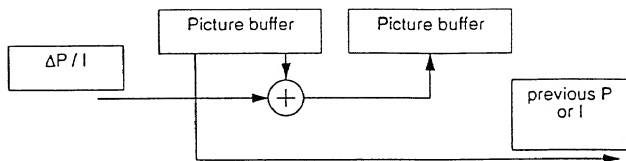


FIG.89

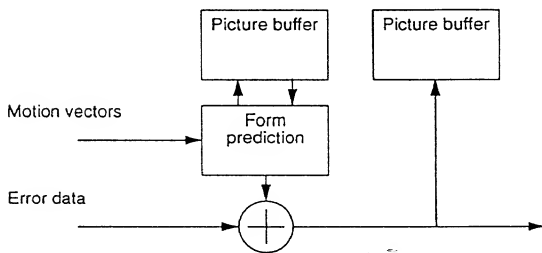


FIG.90

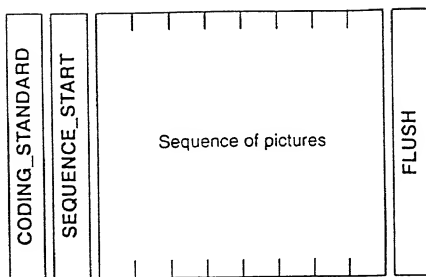


FIG.91

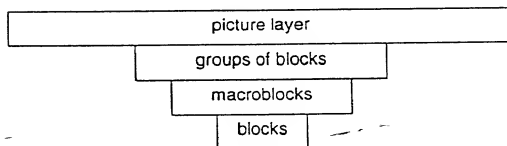


FIG.92

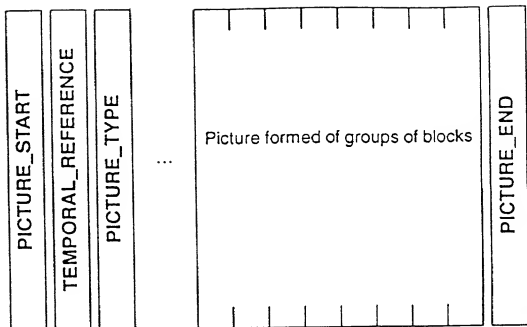


FIG.93

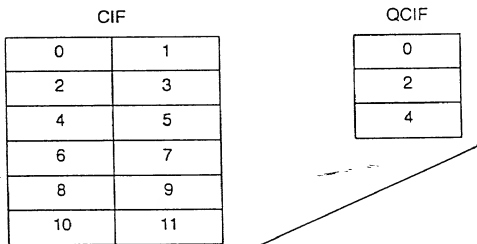


FIG.94

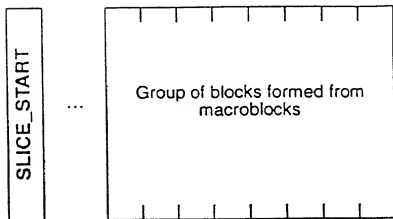


FIG.95

1	2	3	4	5	6	7	8	9	10	11
12	13	14	15	16	17	18	19	20	21	22
23	24	25	26	27	28	29	30	31	32	33

FIG.96

1	2	3	4	5	6	7	8
9	10	11	12	13	14	15	16

...

59	58	59	60	61	62	63	64
----	----	----	----	----	----	----	----

FIG. 99

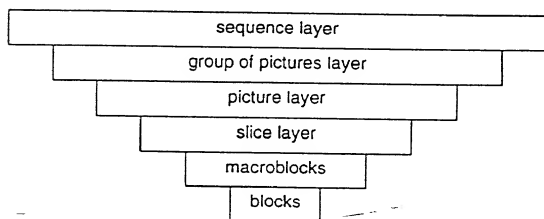


FIG. 100

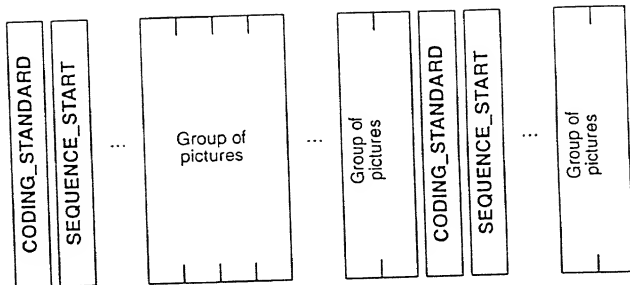


FIG. 101

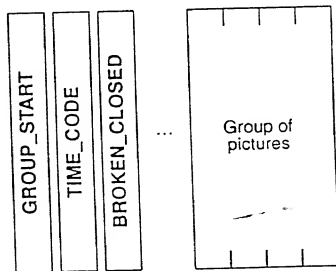


FIG. 102

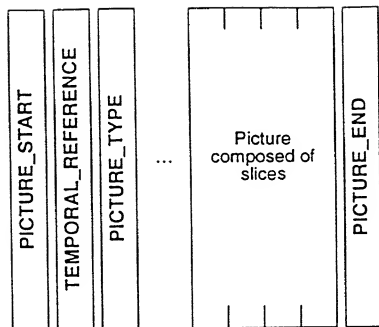


FIG. 103

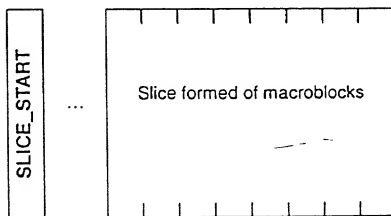


FIG. 104

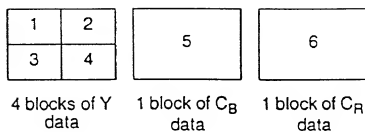


FIG. 105

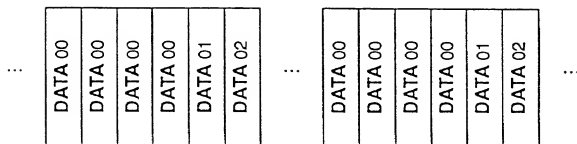


FIG. 106

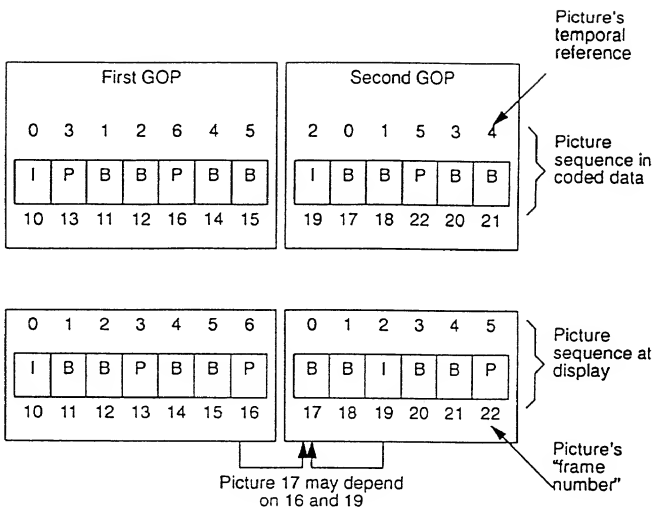


FIG. 107



Access Start

Data Transfer

Default State

FIG. 108

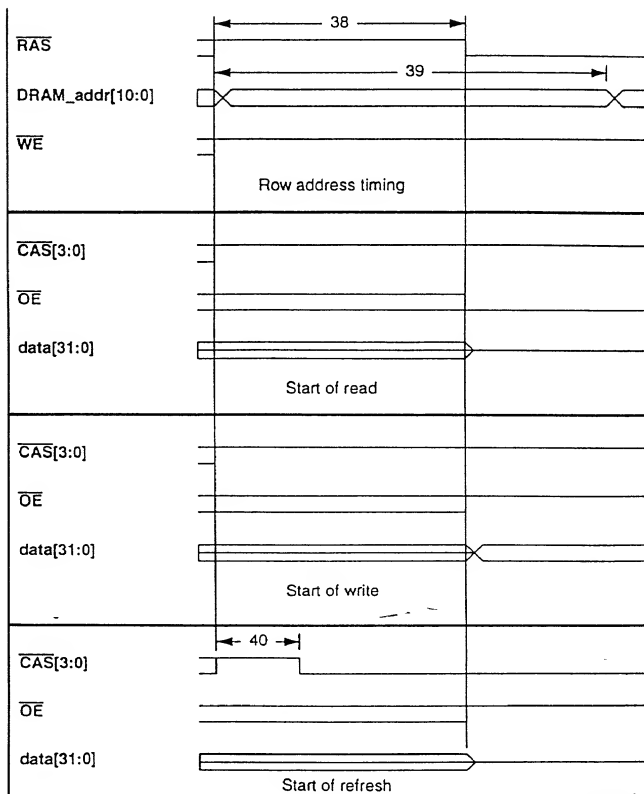


FIG. 109

TIME

RAS

DRAM_addr[10:0]

CAS[3:0]

WE

OE

DRAM_data[31:0]

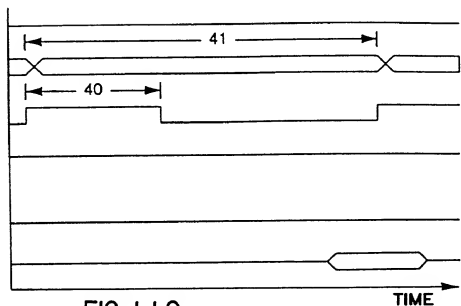


FIG. 110

RAS

DRAM_addr[10:0]

CAS[3:0]

WE

OE

DRAM_data[31:0]

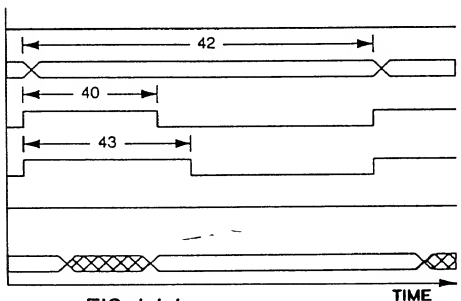


FIG. 111

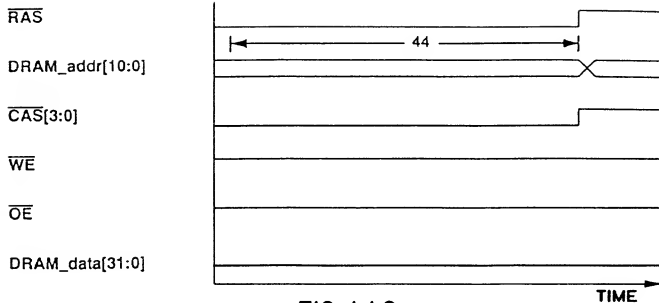


FIG. 1 | 2

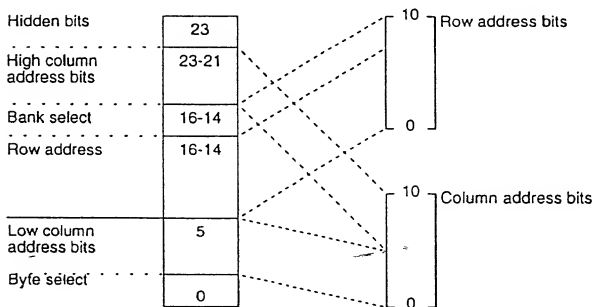


FIG. 1 | 3

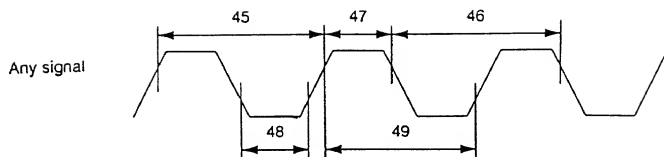


FIG. 114

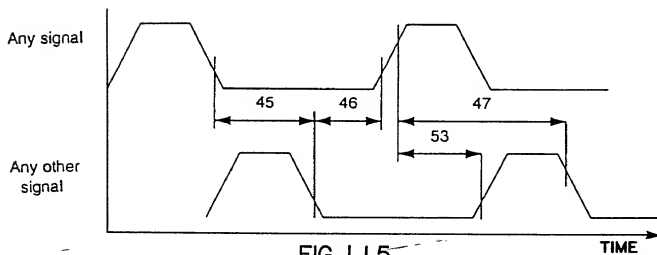
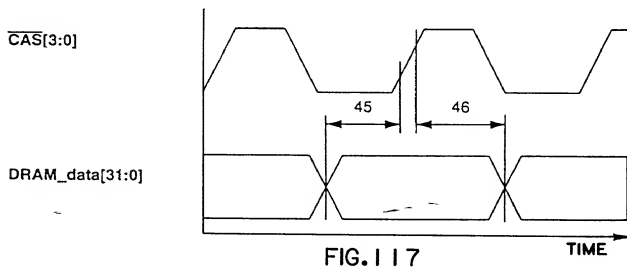
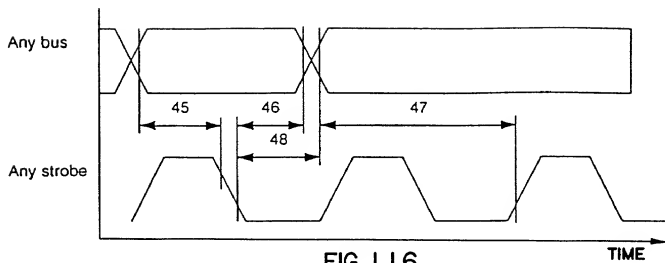


FIG. 115



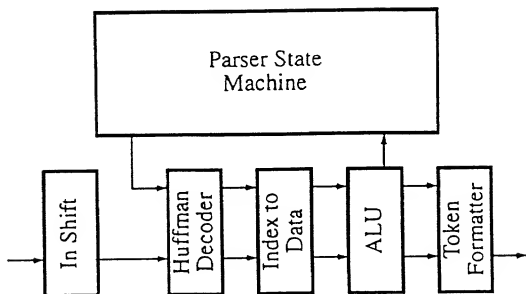


FIG. 118

```

graph TD
    Start([Read AC Coefficients]) --> Decode[Decode Tcoeff VLC]
    Decode --> Escape{Index = ESCAPE ?}
    Escape -- Y --> Read6[Read 6 bit FLC]
    Read6 --> Read1[Read 1 bit FLC]
    Read1 --> Zero1{0 ?}
    Zero1 -- Y --> Read7_1[Read 7 bit FLC]
    Zero1 -- N --> Read7_2[Read 7 bit FLC]
    Read7_1 --> Zero2{0 ?}
    Zero2 -- Y --> Read8_1[Read 8 bit FLC]
    Zero2 -- N --> Read8_2[Read 8 bit FLC]
    Read7_2 --> Zero3{0 ?}
    Zero3 -- Y --> Read8_3[Read 8 bit FLC]
    Zero3 -- N --> Read8_4[Read 8 bit FLC]
    Read8_1 --> Accept([Accept New Command])
    Read8_2 --> Accept
    Read8_3 --> Accept
    Read8_4 --> Accept
    Read8_4 --> Decode
    Read8_3 --> Decode
    Read8_2 --> Decode
    Read8_1 --> Decode
    Read1 --> Accept
    Escape -- N --> EOB{Index = EOB ?}
    EOB -- Y --> Accept
    EOB -- N --> Read1_2[Read 1 bit FLC]
    Read1_2 --> Accept
    
```

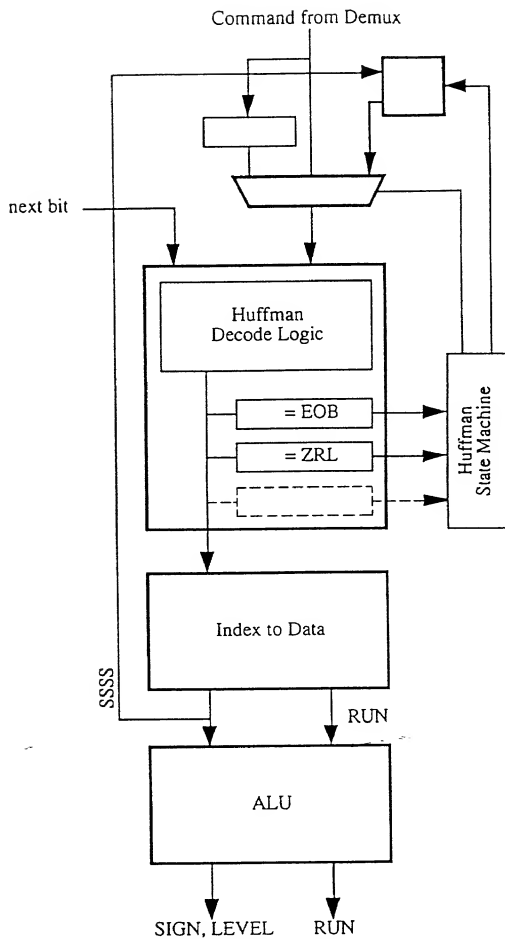


FIG. 120

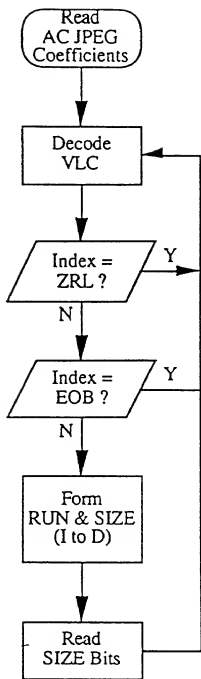


FIG. 121A

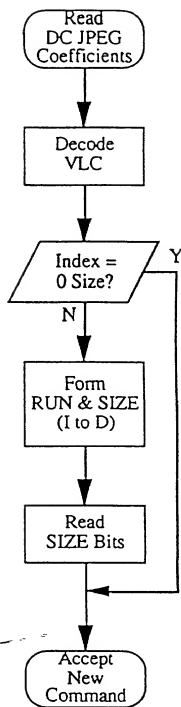


FIG. 121B

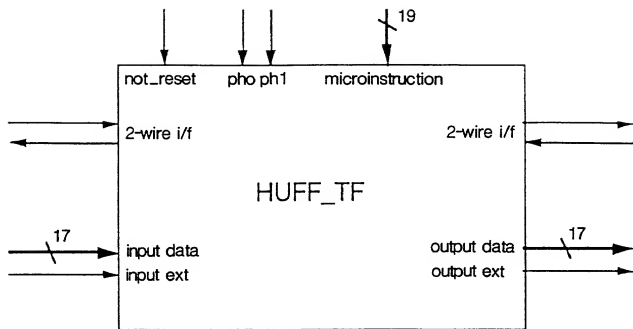


FIG. I 22

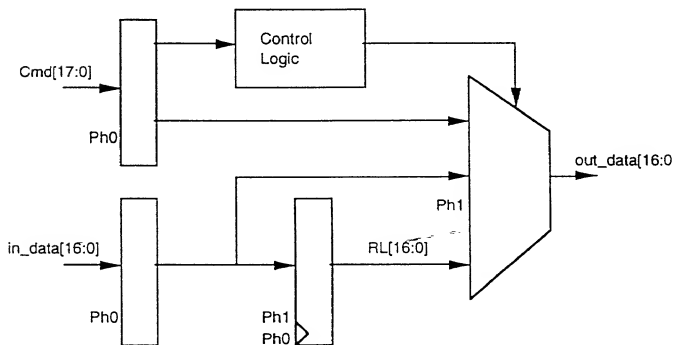


FIG. I 23

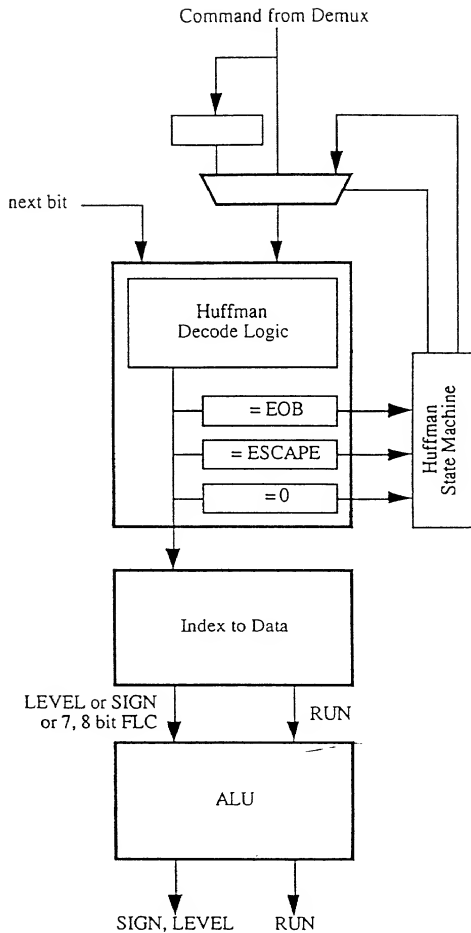


FIG. 124

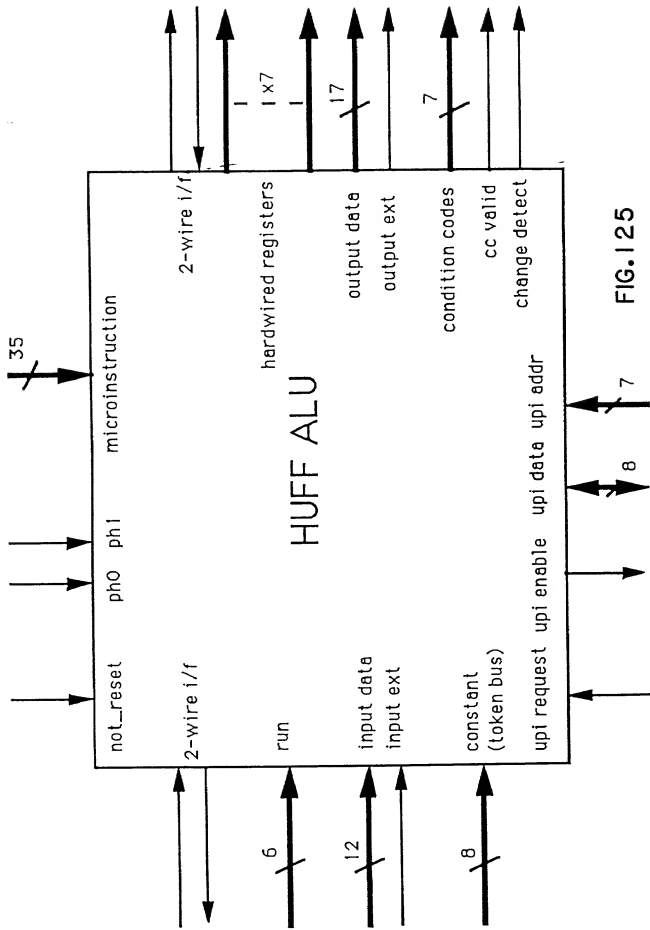


FIG. 125

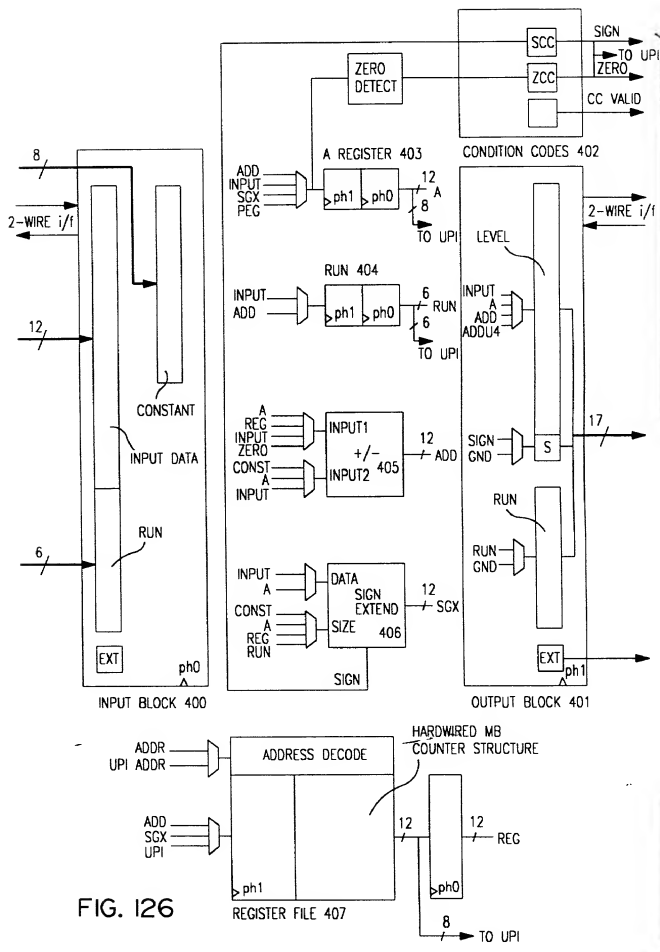


FIG. 126

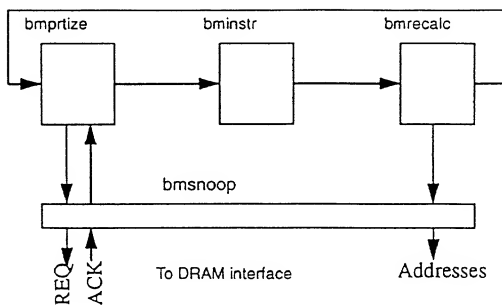


FIG. 127

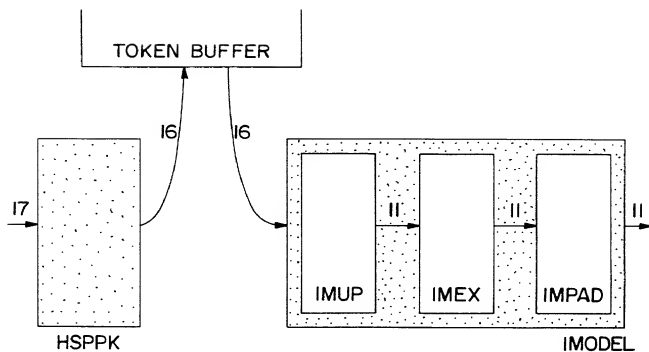


FIG. 1 28

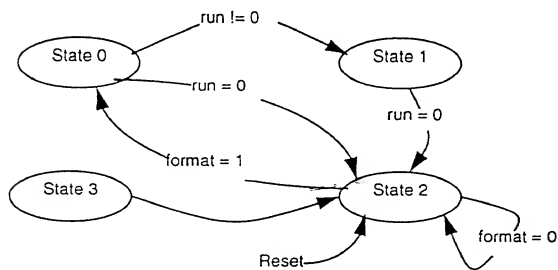


FIG. 1 29

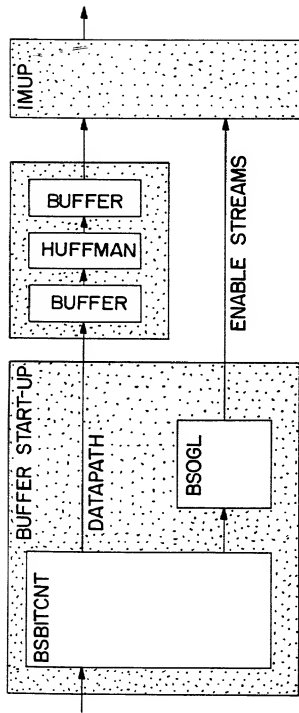


FIG. 130

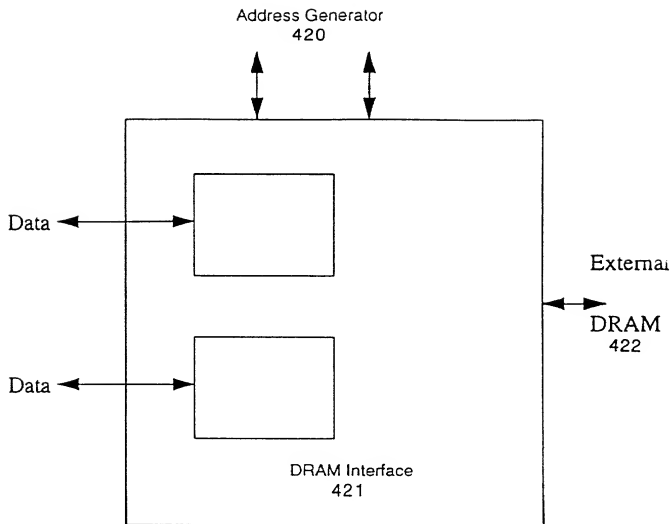


FIG. 131

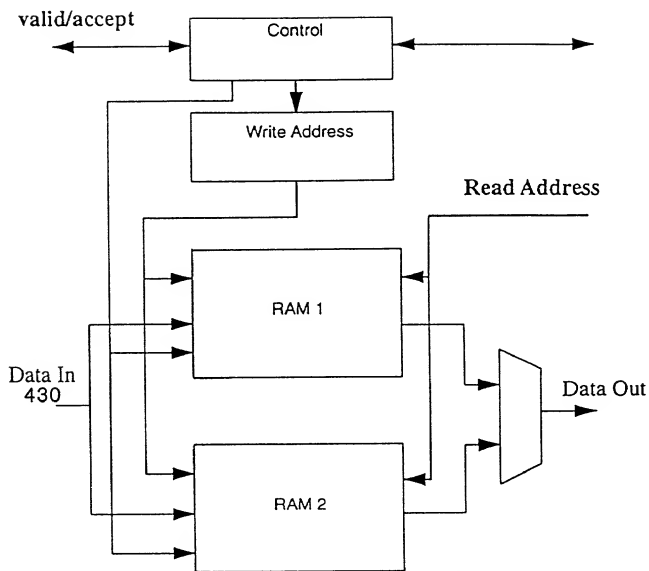


FIG. I 32

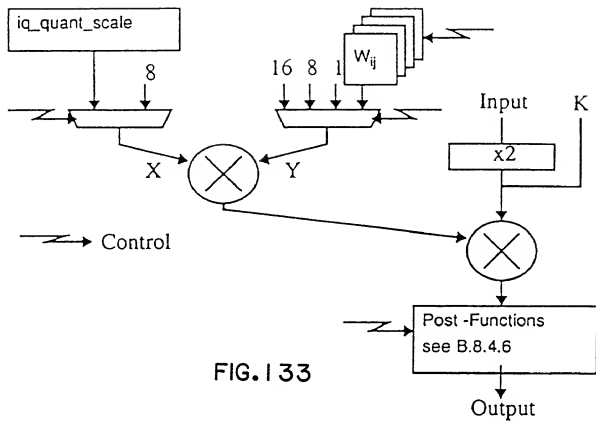


FIG. 133

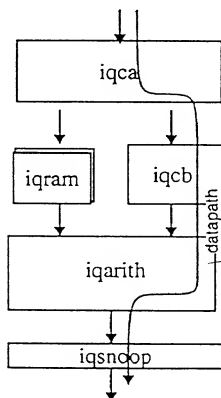


FIG. 134

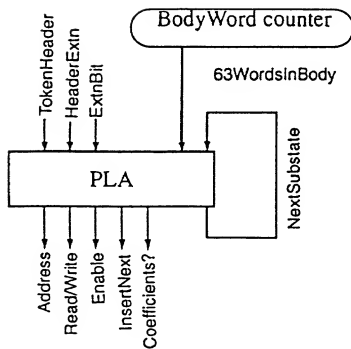


FIG. 1 35

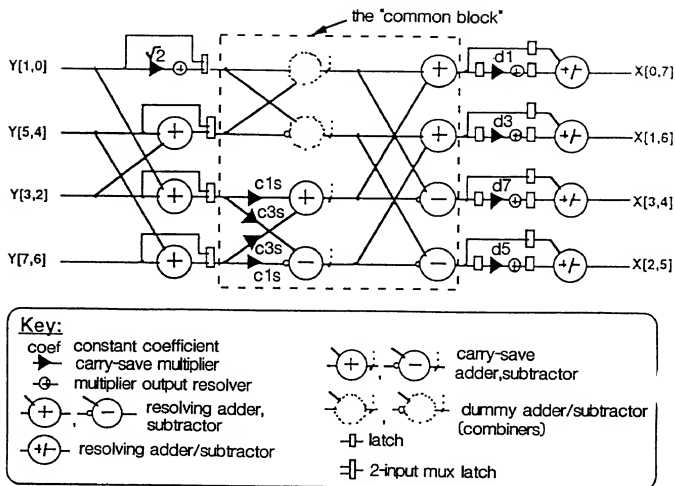


FIG. 137

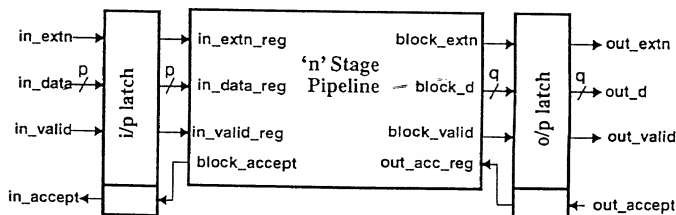
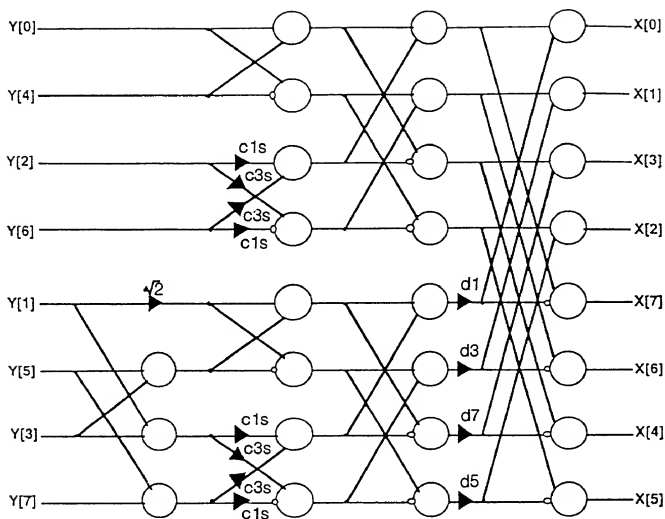


FIG. 138



Key:-

coef
constant coefficient multiplier

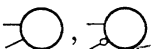


FIG. I 36

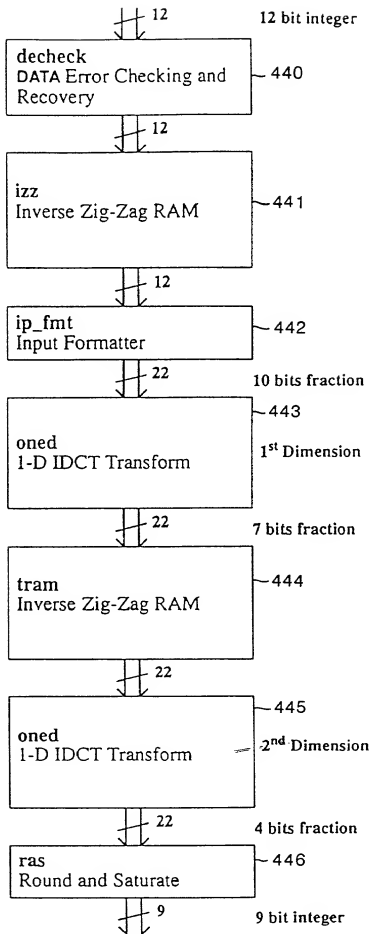


FIG. 139

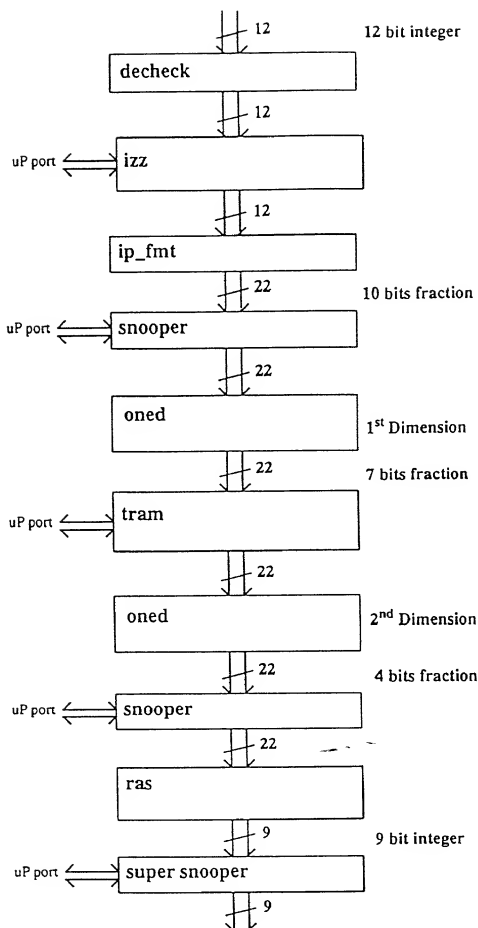
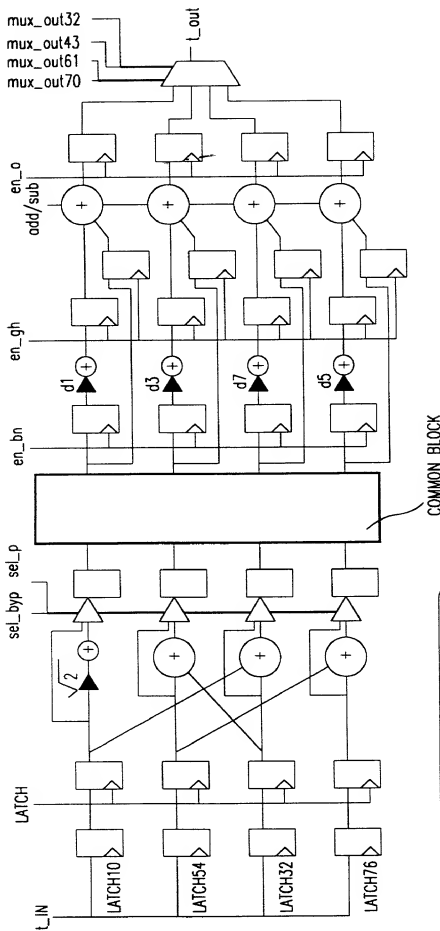


FIG. 140



NOTE: "COMMON BLOCK" IS ENTIRELY COMBINATIONAL (NO LATCHING)

FIG. 14I

0375641-1130303

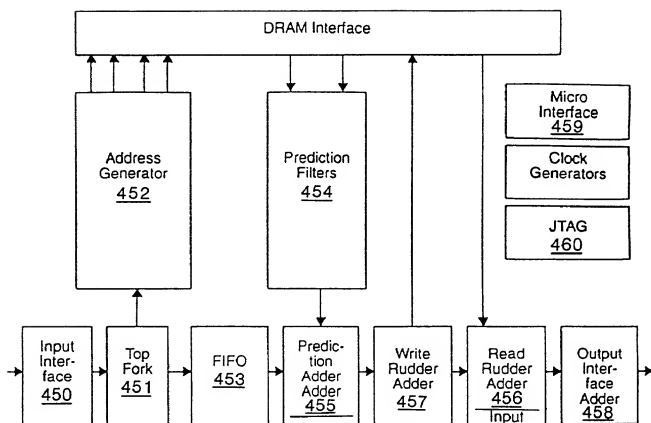


FIG. 142

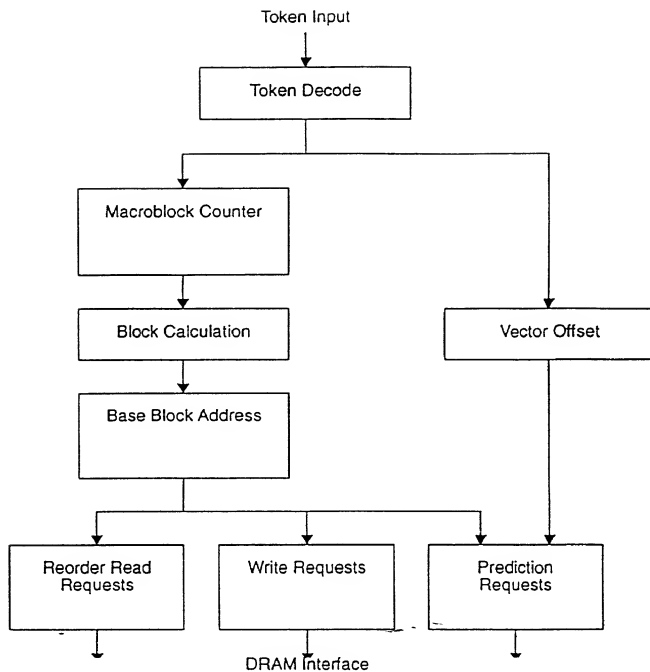


FIG. 144

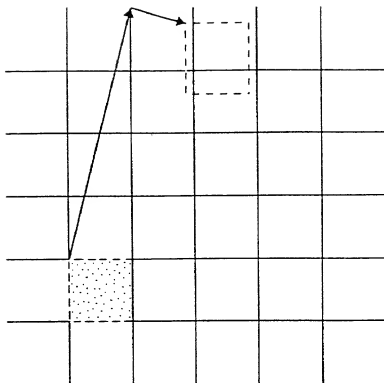


FIG. 145

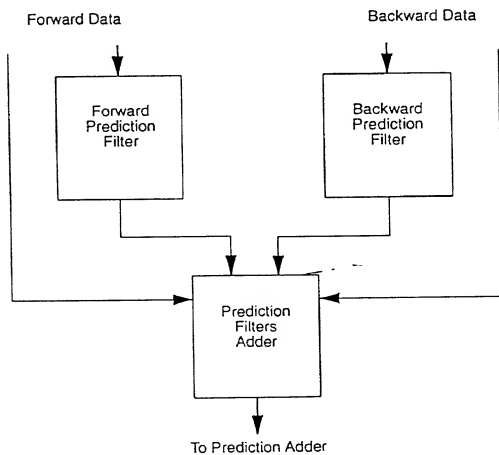


FIG. 146

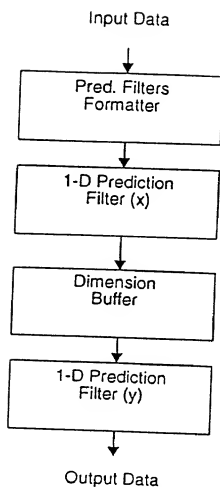


FIG. 147

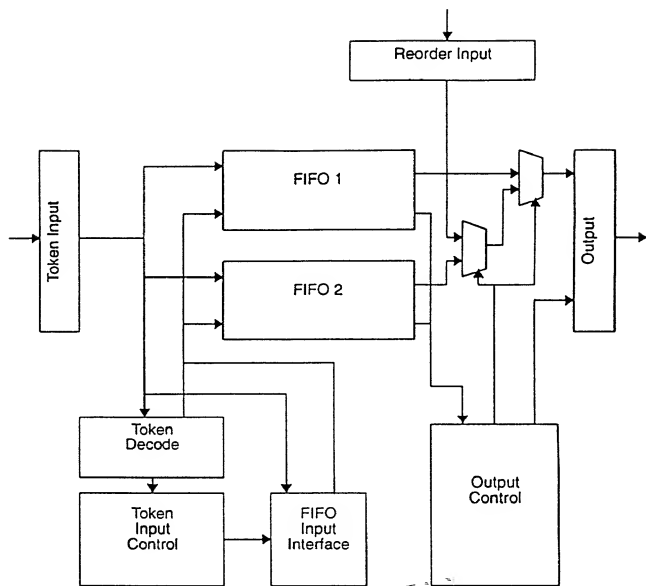


FIG. 150

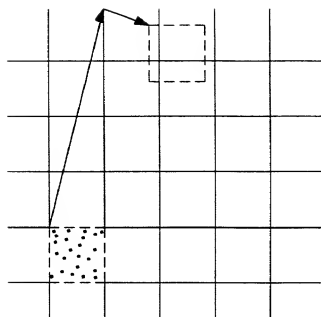


FIG. 151

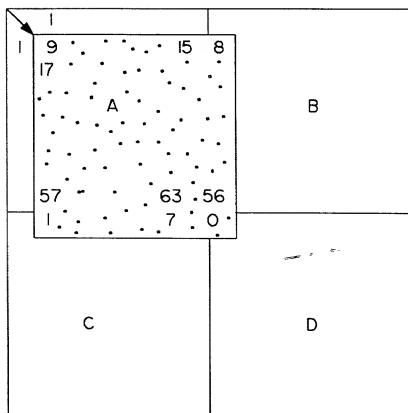


FIG. 152

Read Cycle

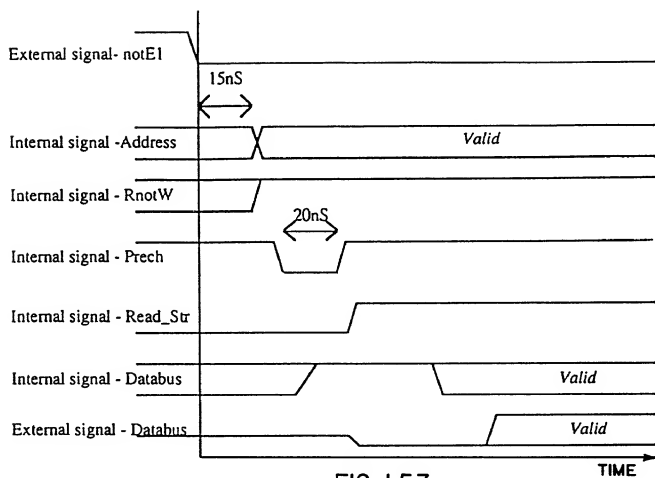


FIG. 153 -

Write Cycle

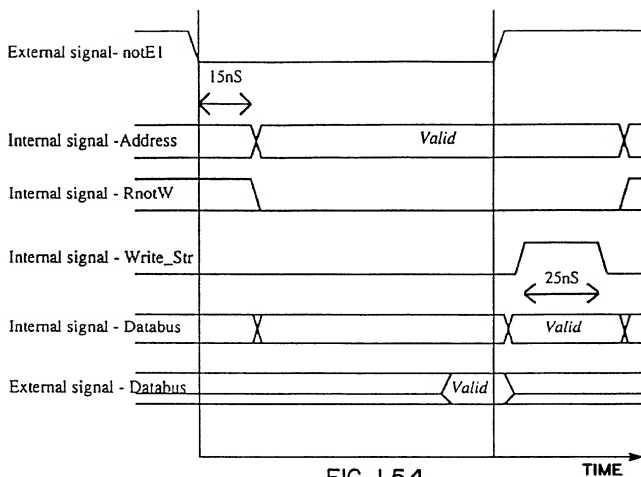
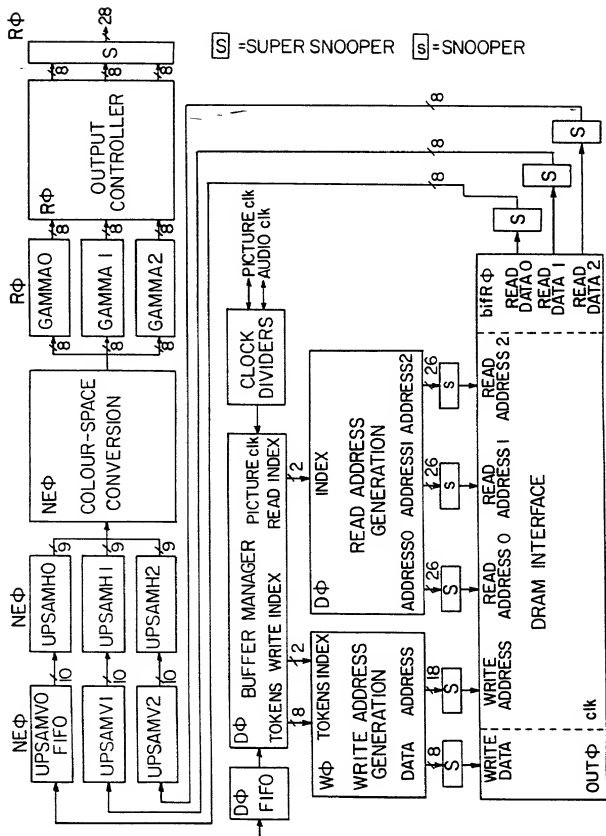


FIG. 154



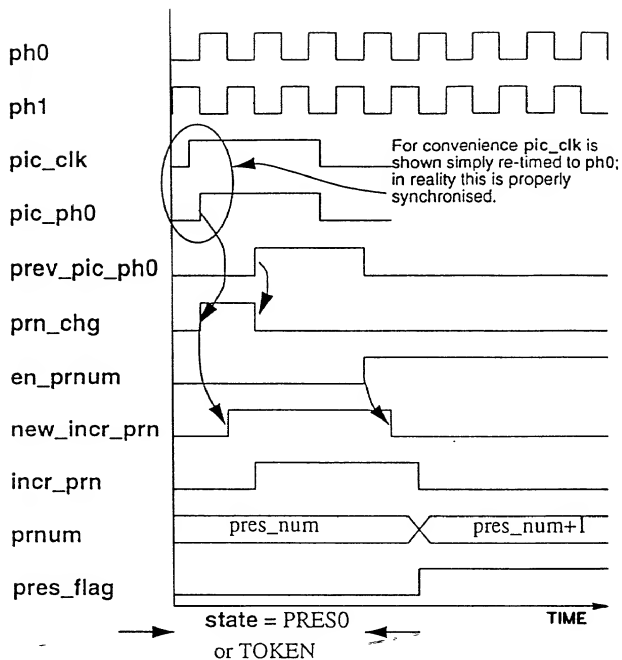


FIG. 156

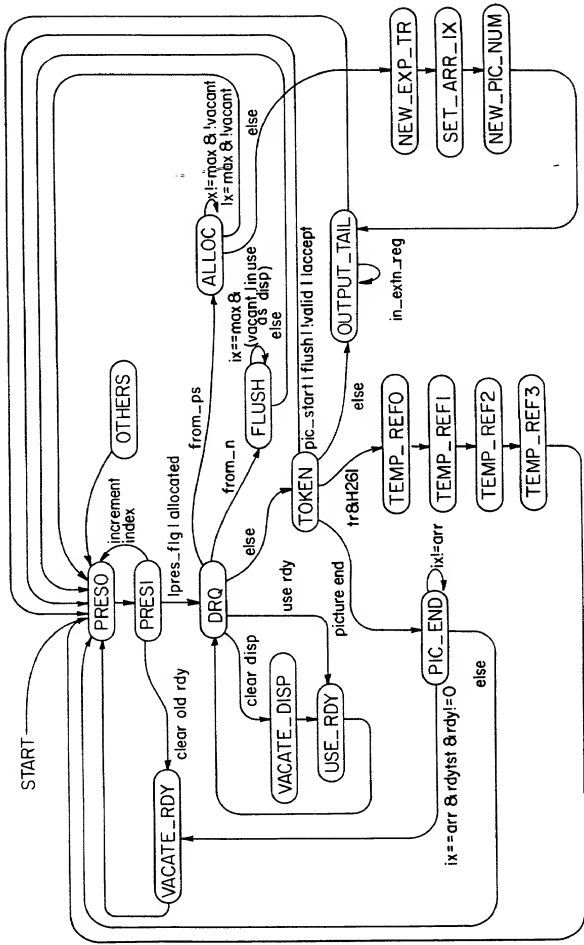


FIG. 157

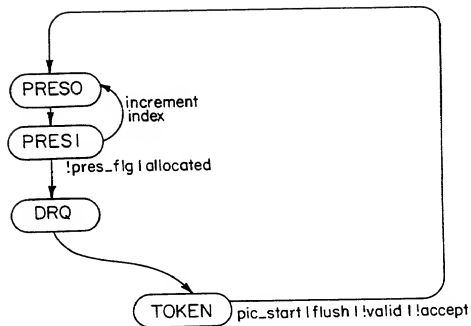


FIG. 158

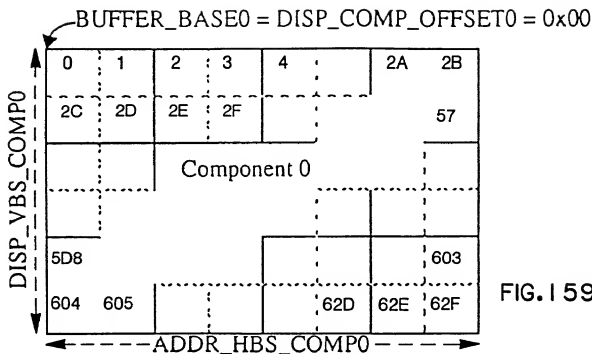


FIG. 159A

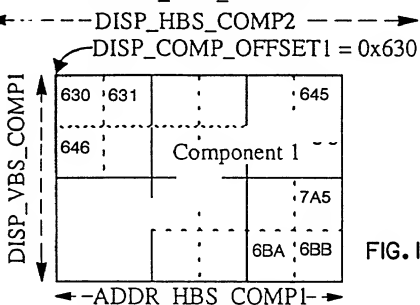


FIG. 159B

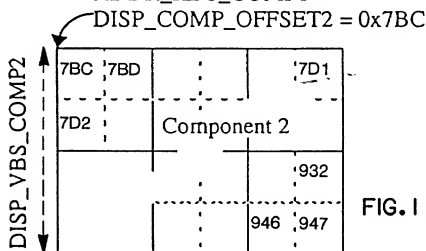


FIG. 159C

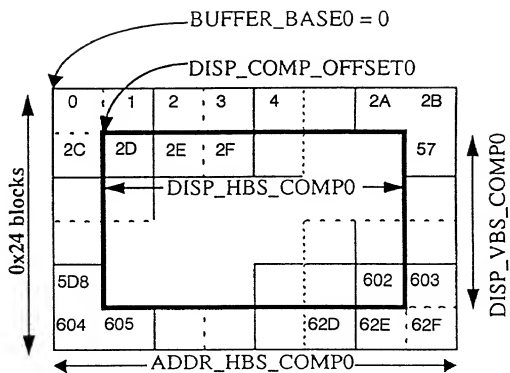


FIG. 160

NOTES

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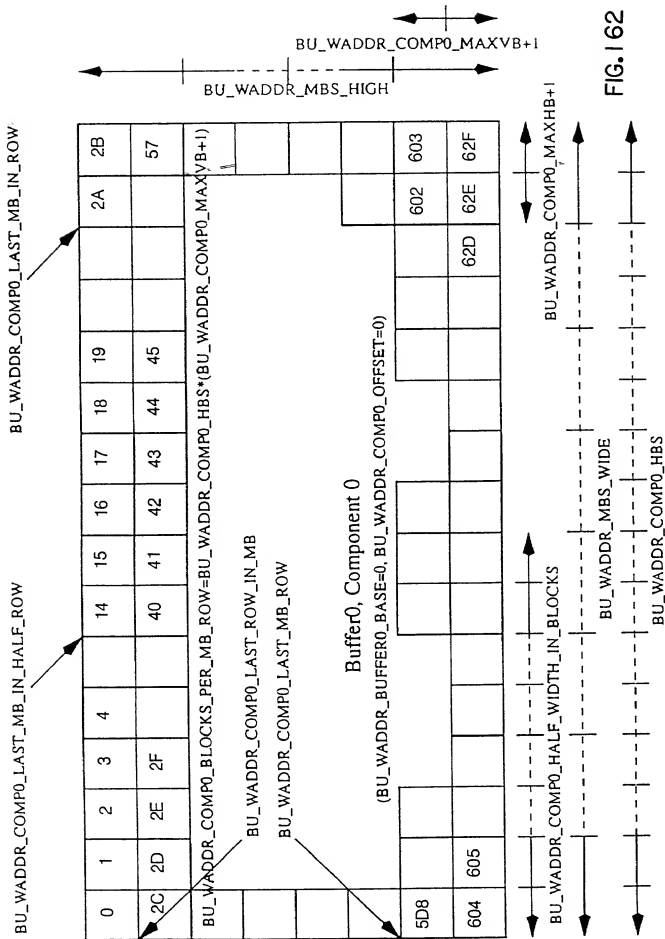
NOTES

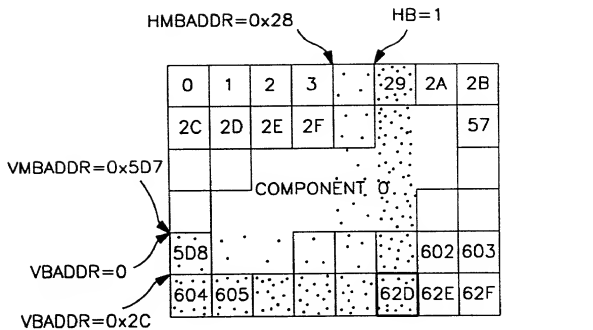
NOTES

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NOTES

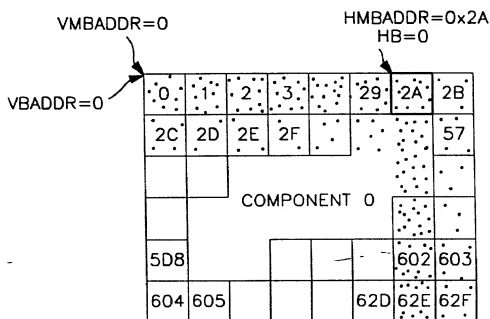
NOTES





$$\text{BLOCK ADDRESS} = 0 + 0 + 0 + 0x5D8 + 0x28 + 0x2C + 1 = 0x62D$$

FIG. I 63A



$$\text{BLOCK ADDRESS} = 0 + 0 + 0 + 0x2A + 0 + 0 = 0x2A$$

FIG. I 63B

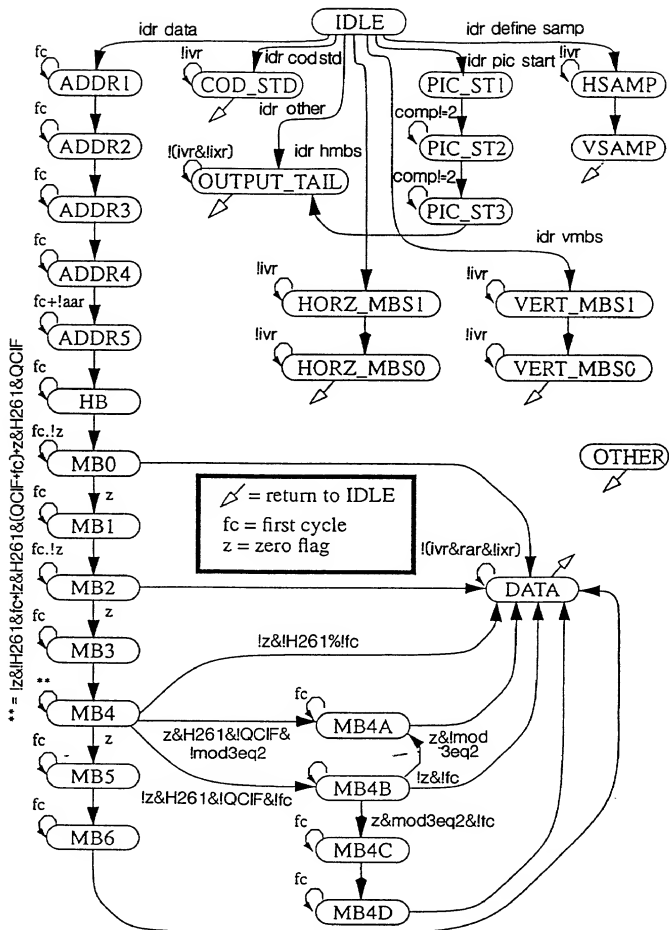


FIG. 164

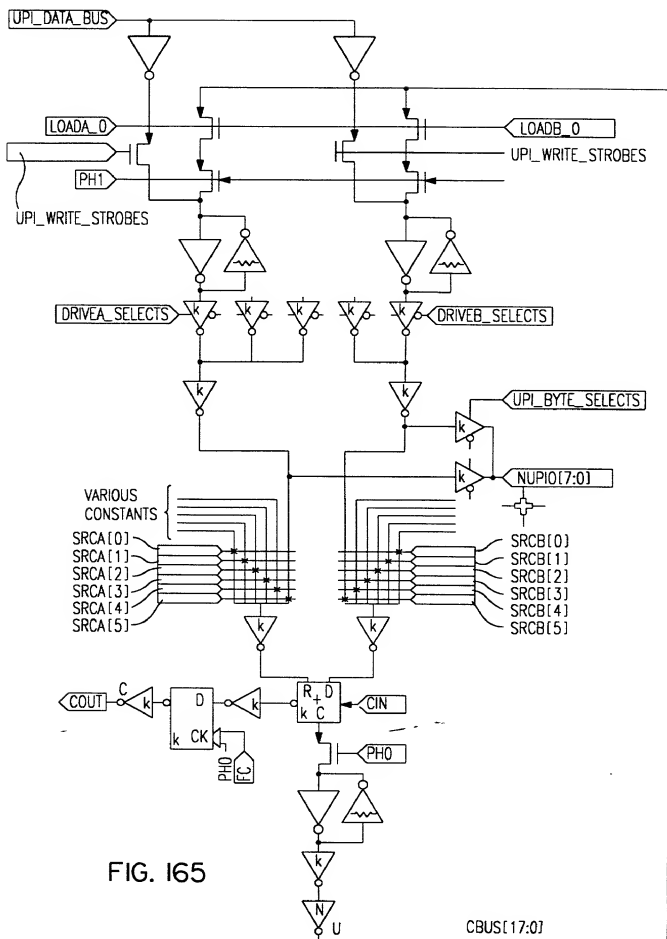
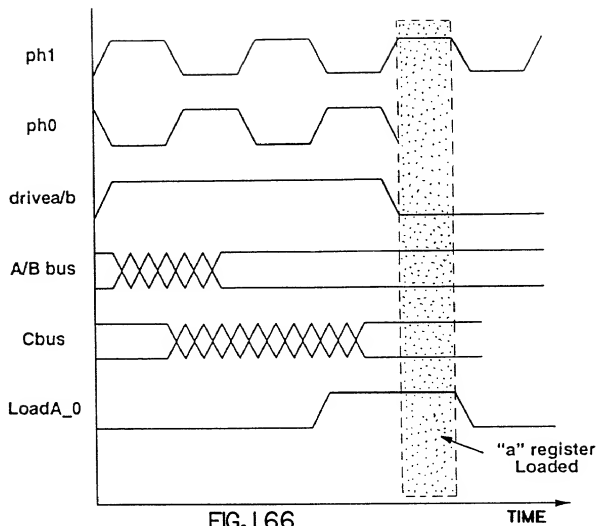


FIG. 165

CBUS[17:0]



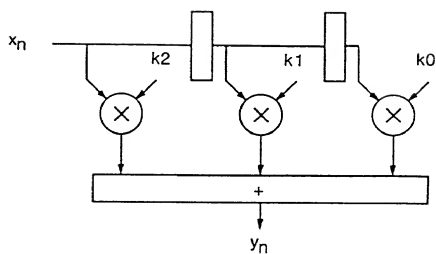


FIG. 167

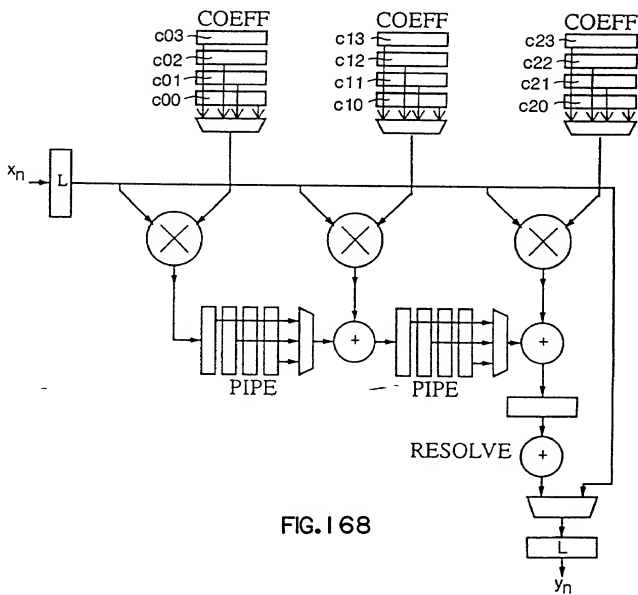


FIG. 168

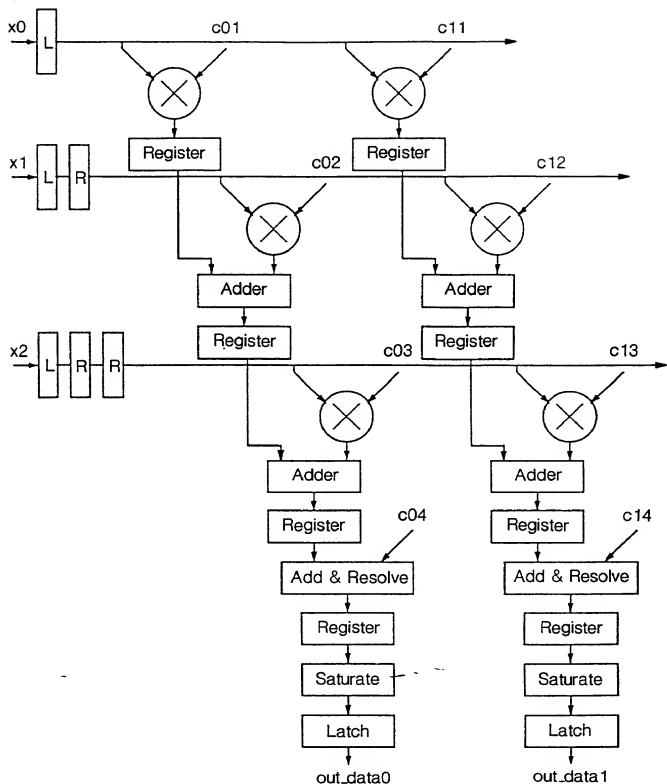


FIG. 169